Lampiran 1. Datasheet BH1750FVI

● Descriptions

BH1750FVI is an digital Ambient Light Sensor IC for I^2C bus interface. This IC is the most suitable to obtain the ambient light data for adjusting LCD and Keypad backlight power of Mobile phone. It is possible to detect wide range at High resolution.
(1 - 65535 lx).

● Features

1) I^2C bus Interface (f / s Mode Support)
2) Spectral responsibility is approximately human eye response
3) Illuminance to Digital Converter
4) Wide range and High resolution. (1 - 65535 lx)
5) Low Current by power down function
6) 50Hz / 60Hz Light noise reject-function
7) 1.8V Logic input interface
8) No need any external parts
9) Light source dependency is little. (ex. Incandescent Lamp. Fluorescent Lamp. Halogen Lamp. White LED. Sun Light)
10) It is possible to select 2 type of I^2C slave-address.
11) Adjustable measurement result for influence of optical window
(It is possible to detect min. 0.11 lx, max. 100000 lx by using this function.)
12) Small measurement variation (+/- 20%)
13) The influence of infrared is very small.

● Applications

Mobile phone, LCD TV, NOTE PC, Portable game machine, Digital camera, Digital video camera, Car navigation, PDA, LCD display

● Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	Vmax	4.5	V
Operating Temperature	Topr	-40～85	℃
Storage Temperature	Tstg	-40～100	℃
SDA Sink Current	Imax	7	mA
Power Dissipation	Pd	260※	mW

※ 70mm × 70mm × 1.6mm glass epoxy board. Derating in done at 3.47mW/℃ for operating above Ta=25℃.

● Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Vcc Voltage	Vcc	2.4	3.0	3.6	V
I^2C Reference Voltage	VDVI	1.65	-	Vcc	V

Ambient Light Sensor IC Series

Digital 16bit Serial Output Type Ambient Light Sensor IC

BH1750FVI

No.09046EBT01

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●Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Vcc Voltage	Vcc	2.4	3.0	3.6	V
I^2C Reference Voltage	VDVI	1.65	-	Vcc	V

●Electrical Characteristics (V_{CC} = 3.0V, DVI = 3.0V, Ta = 25℃, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current	Icc1	—	120	190	μA	Ev = 100 lx ※1
Powerdown Current	Icc2	—	0.01	1.0	μA	No input Light
Peak Wave Length	λp	—	560	—	nm	
Measurement Accuracy	S/A	0.96	1.2	1.44	times	Sensor out / Actual lx EV = 1000 lx ※1, ※2
Dark (0 lx) Sensor out	S0	0	0	3	count	H-Resolution Mode ※3
H-Resolution Mode Resolution	r_{HR}	—	1	—	lx	
L-Resolution Mode Resolution	r_{LR}	—	4	—	lx	
H-Resolution Mode Measurement Time	t_{HR}	—	120	180	ms	
L-Resolution Mode Measurement Time	t_{LR}	—	16	24	ms	
Incandescent / Fluorescent Sensor out ratio	r_{IF}	—	1	—	times	EV = 1000 lx
ADDR Input ‘H’ Voltage	V_{AH}	0.7 * VCC	—	—	V	
ADDR Input ‘L’ Voltage	V_{AL}	—	—	0.3 * VCC	V	
DVI Input ‘L’ Voltage	V_{DVL}	—	—	0.4	V	
SCL, SDA Input ‘H’ Voltage 1	$V_{IH}1$	0.7 * DVI	—	—	V	DVI ≧ 1.8V
SCL, SDA Input ‘H’ Voltage 2	$V_{IH}2$	1.26	—	—	V	1.65V ≦ DVI ＜1.8V
SCL, SDA Input ‘L’ Voltage 1	$V_{IL}1$	—	—	0.3 * DVI	V	DVI ≧ 1.8V
SCL, SDA Input ‘L’ Voltage 2	$V_{IL}2$	—	—	DVI – 1.26	V	1.65V ≦ DVI ＜ 1.8V
SCL, SDA, ADDR Input ‘H’ Current	I_{IH}	—	—	10	μA	
SCL, SDA, ADDR Input ‘L’ Current	I_{IL}	—	—	10	μA	
I^2C SCL Clock Frequency	f_{SCL}	—	—	400	kHz	
I^2C Bus Free Time	t_{BUF}	1.3	—	—	μs	
I^2C Hold Time (repeated) START Condition	t_{HDSTA}	0.6	—	—	μs	
I^2C Set up time for a Repeated START Condition	t_{SUSTA}	0.6	—	—	μs	
I^2C Set up time for a Repeated STOP Condition	t_{SUSTD}	0.6	—	—	μs	
I^2C Data Hold Time	t_{HDDAT}	0	—	0.9	μs	
I^2C Data Setup Time	t_{SUDAT}	100	—	—	ns	
I^2C ‘L’ Period of the SCL Clock	t_{LOW}	1.3	—	—	μs	
I^2C ‘H’ Period of the SCL Clock	t_{HIGH}	0.6	—	—	μs	
I^2C SDA Output ‘L’ Voltage	V_{OL}	0	—	0.4	V	I_{OL} = 3 mA

※1 White LED is used as optical source.
※2 Measurement Accuracy typical value is possible to change '1' by "Measurement result adjustment function".
※3 Use H-resolution mode or H-resolution mode2 if dark data (less than 10 lx) is need.

●Reference Data

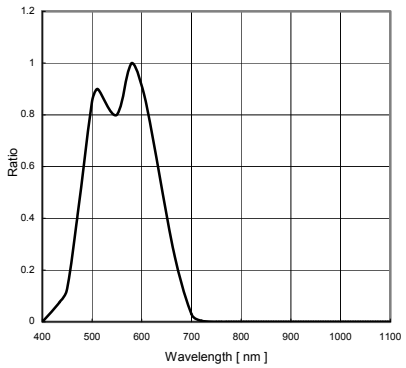


Fig.1 Spectral Response

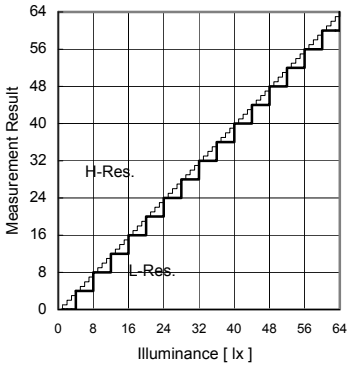


Fig.2 Illuminance - Measurement Result 1

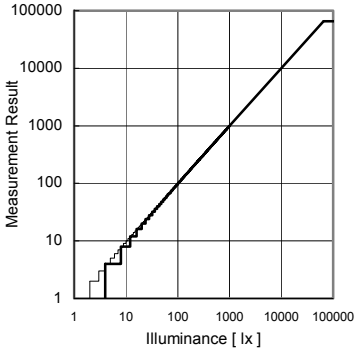


Fig.3 Illuminance - Measuremnet Result 2

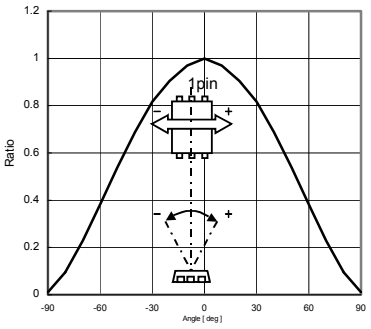


Fig.4 Directional Characteristics 1

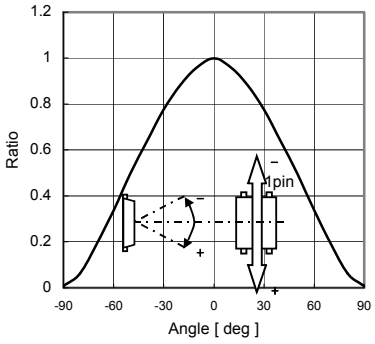


Fig.5 Directional Characteristics 2

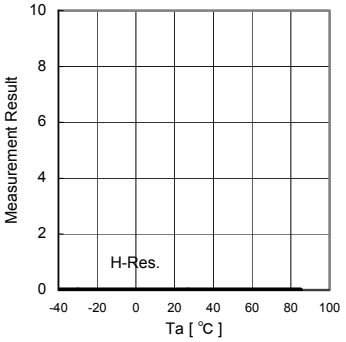


Fig.6 Dark Response

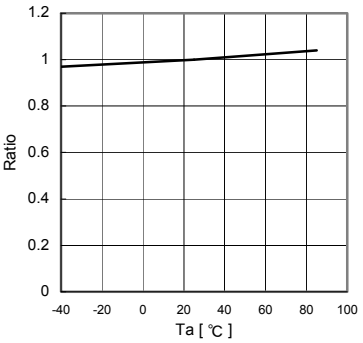


Fig.7 Measurement Accuracy Temperature Dependency

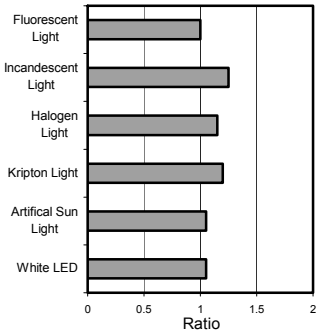


Fig.8 Light Source Dependency (Fluorescent Light is set to '1')

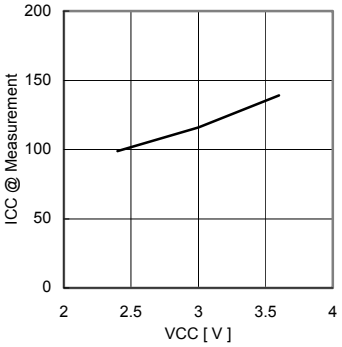


Fig.9 VCC - ICC (During measurement)

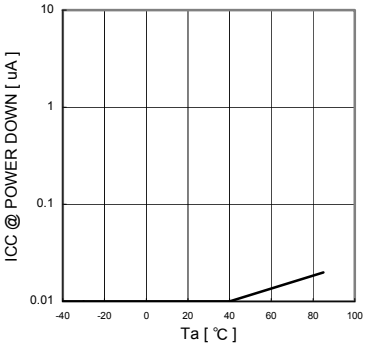


Fig.10 VCC – ICC@0 Lx (POWER DOWN)

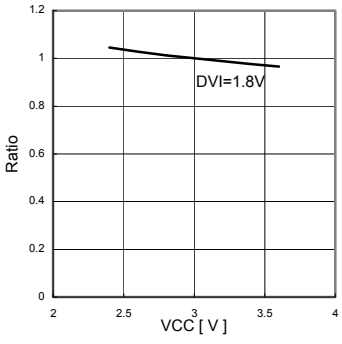


Fig.11 Measurement Result VCC Dependency

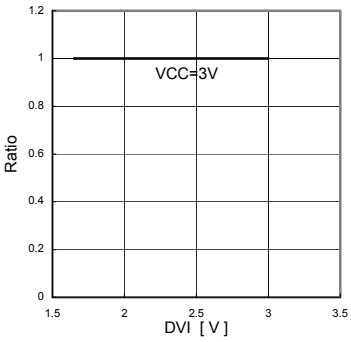
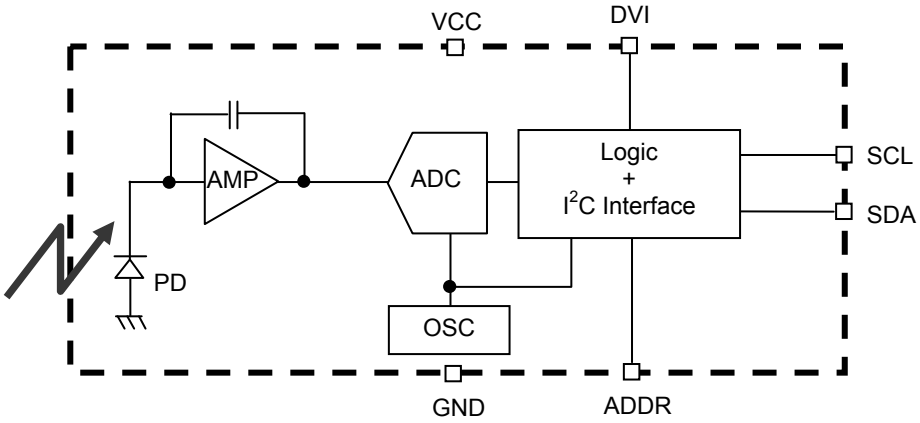


Fig.12 Measurement Result DVI Dependency

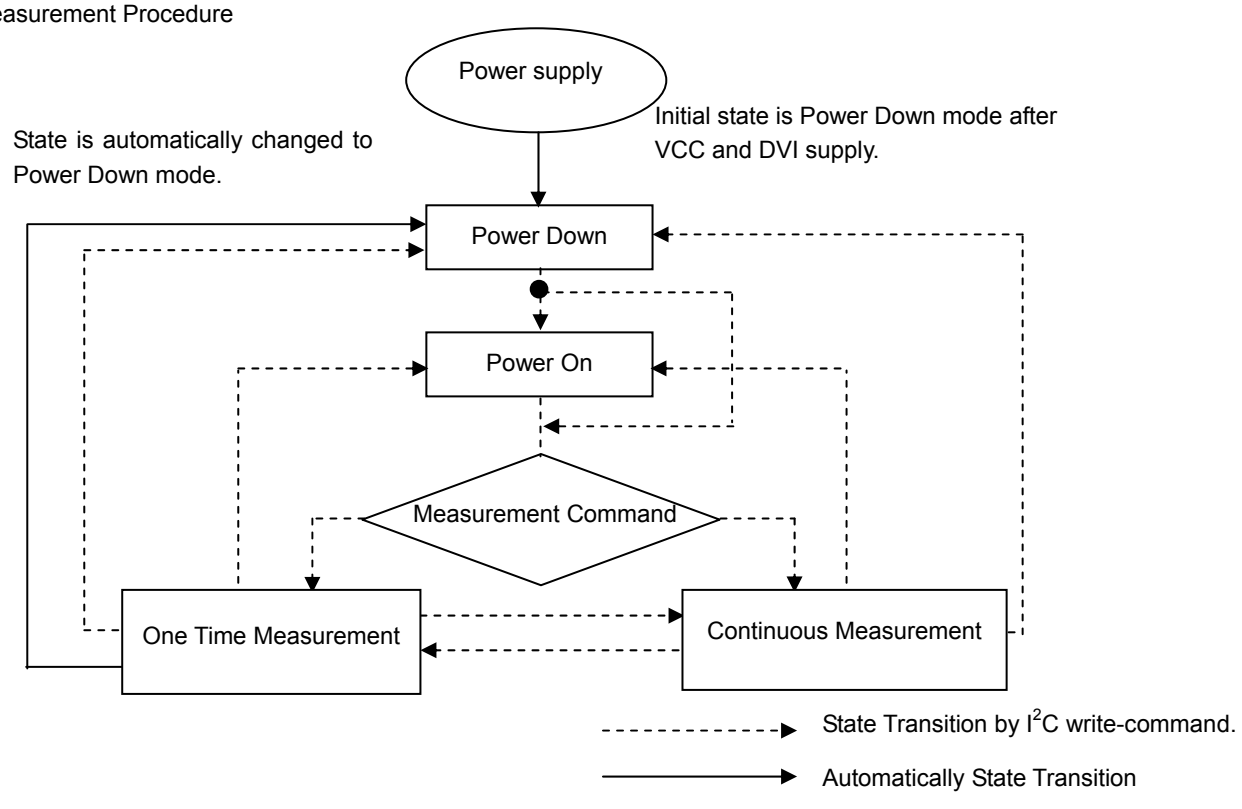
●Block Diagram



●Block Diagram Descriptions

・PD
Photo diode with approximately human eye response.
・AMP
Integration-OPAMP for converting from PD current to Voltage.
・ADC
AD converter for obtainment Digital 16bit data.
・Logic + I^2C Interface
Ambient Light Calculation and I^2C BUS Interface. It is including below register.
Data Register → This is for registration of Ambient Light Data. Initial Value is "0000_0000_0000_0000".
Measurement Time Register → This is for registration of measurement time. Initial Value is "0100_0101".
・OSC
Internal Oscillator (typ. 320kHz). It is CLK for internal logic.

●Measurement Procedure



* "Power On" Command is possible to omit.

●Instruction Set Architecture

Instruction	Opecode	Comments
Power Down	0000_0000	No active state.
Power On	0000_0001	Waiting for measurement command.
Reset	0000_0111	Reset Data register value. Reset command is not acceptable in Power Down mode.
Continuously H-Resolution Mode	0001_0000	Start measurement at 1lx resolution. Measurement Time is typically 120ms.
Continuously H-Resolution Mode2	0001_0001	Start measurement at 0.5lx resolution. Measurement Time is typically 120ms.
Continuously L-Resolution Mode	0001_0011	Start measurement at 4lx resolution. Measurement Time is typically 16ms.
One Time H-Resolution Mode	0010_0000	Start measurement at 1lx resolution. Measurement Time is typically 120ms. It is automatically set to Power Down mode after measurement.
One Time H-Resolution Mode2	0010_0001	Start measurement at 0.5lx resolution. Measurement Time is typically 120ms. It is automatically set to Power Down mode after measurement.
One Time L-Resolution Mode	0010_0011	Start measurement at 4lx resolution. Measurement Time is typically 16ms. It is automatically set to Power Down mode after measurement.
Change Measurement time (High bit)	01000_MT[7,6,5]	Change measurement time. ※ Please refer "adjust measurement result for influence of optical window."
Change Masurement time (Low bit)	011_MT[4,3,2,1,0]	Change measurement time. ※ Please refer "adjust measurement result for influence of optical window."

※ Don't input the other opecode.

●Measurement mode explanation

Measurement Mode	Measurement Time.	Resolurtion
H-resolution Mode2	Typ. 120ms.	0.5 lx
H-Resolution Mode	Typ. 120ms.	1 lx.
L-Resolution Mode	Typ. 16ms.	4 lx.

We recommend to use H-Resolution Mode.
Measurement time (integration time) of H-Resolution Mode is so long that some kind of noise(including in 50Hz / 60Hz noise) is rejected. And H-Resolution Mode is 1 l x resolution so that it is suitable for darkness (less than 10 lx)
H-resolution mode2 is also suitable to detect for darkness.

●Explanation of Asynchronous reset and Reset command "0000_0111"

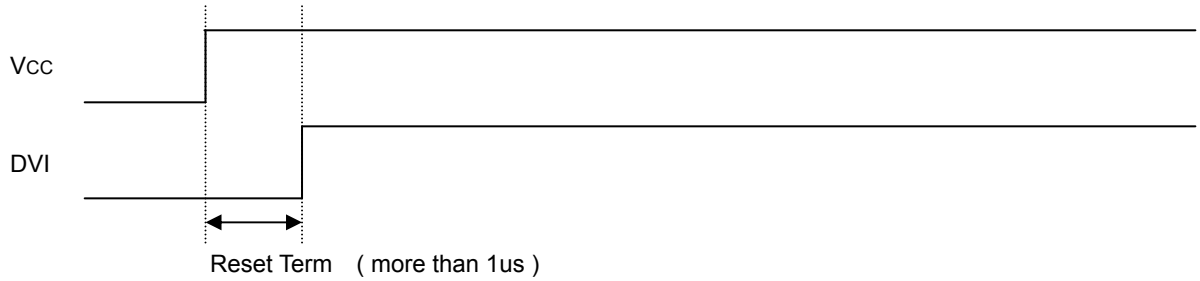
1) Asynchronous reset
All registers are reset. It is necessary on power supply sequence. Please refer "Timing chart for VCC and DVI power supply sequence" in this page. It is power down mode during DVI = 'L'.

2) Reset command
Reset command is for only reset Illuminance data register. (reset value is '0') It is not necessary even power supply sequence.It is used for removing previous measurement result. This command is not working in power down mode, so that please set the power on mode before input this command.

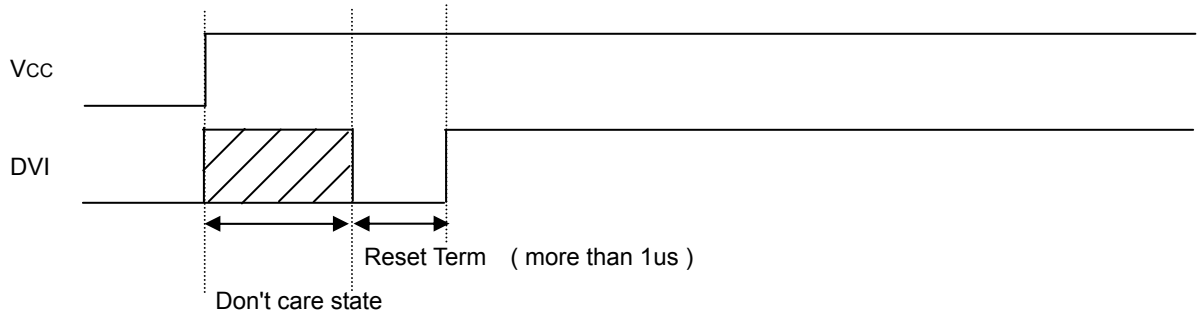
●Timing chart for VCC and DVI power supply sequence

DVI is I^2C bus reference voltage terminal. And it is also asynchronous reset terminal. It is necessary to set to 'L' after VCC is supplied. In DVI 'L' term, internal state is set to Power Down mode.

1) Recommended Timing chart1 for VCC and DVI supply.



2) Timing chart2 for VCC and DVI supply.
(If DVI rises within 1μs after VCC supply)



Don't care state
ADDR, SDA, SCL is not stable if DVI 'L' term (1us) is not given by systems.
In this case, please connect the resisters (approximately 100kOhm) to ADDR without directly connecting to VCC or GND,
because it is 3 state buffer for Internal testing.

●Measurement sequence example from "Write instruction" to "Read measurement result"

ex1) Continuously H-resolution mode (ADDR = 'L')

from Master to Slave

from Slave to Master

① Send "Continuously H-resolution mode " instruction

ST	0100011	0	Ack	00010000	Ack	SP

② Wait to complete 1st H-resolution mode measurement.(max. 180ms.)

③ Read measurement result.

ST	0100011	1	Ack	High Byte [15:8]	Ack

Low Byte [7:0]	$\overline{\text{Ack}}$	SP

How to calculate when the data High Byte is "10000011" and Low Byte is "10010000"
$(2^{15} + 2^{9} + 2^{8} + 2^{7} + 2^{4}) / 1.2 \fallingdotseq 28067$ [lx]

The result of continuously measurement mode is updated.(120ms.typ at H-resolution mode, 16ms.typ at L-resolution mode)

ex2) One time L-resolution mode (ADDR = 'H')

① Send "One time L-resolution mode " instruction

ST	1011100	0	Ack	00100011	Ack	SP

② Wait to complete L-resolution mode measurement.(max. 24ms.)

③ Read measurement result

ST	1011100	1	Ack	High Byte [15:8]	Ack

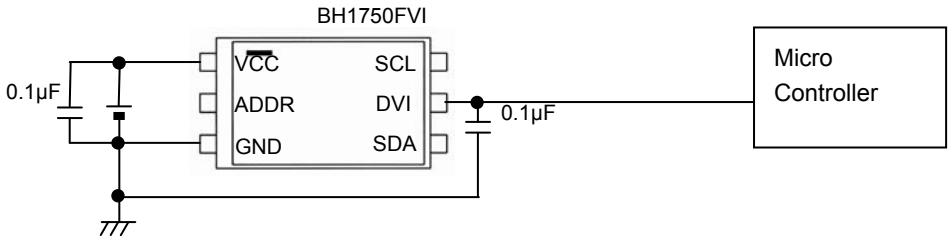
Low Byte [7:0]	$\overline{\text{Ack}}$	SP

How to calculate when the data High Byte is "00000001" and Low Byte is "00010000"
$(2^{8} + 2^{4}) / 1.2 \fallingdotseq 227$ [lx]
In one time measurement, Statement moves to power down mode after measurement completion.If updated result is need then please resend measurement instruction.

●Application circuit example of DVI terminal

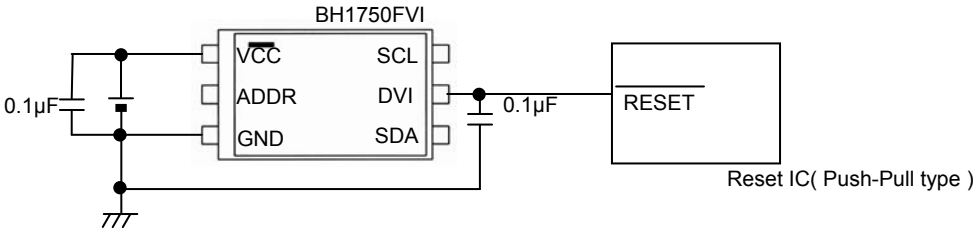
The DVI terminal is an asynchronous reset terminal. Please note that there is a possibility that IC doesn't operate normally if the reset section is not installed after the start-up of VCC.
(Please refer to the paragraph of "Timing chart for VCC and DVI power supply sequence")
The description concerning SDA and the terminal SCL is omitted in this application circuit example. Please design the application the standard of the I2C bus as it finishes being satisfactory. Moreover, the description concerning the terminal ADDR is omitted. Please refer to the paragraph of "Timing chart for VCC and DVI power supply sequence" about the terminal ADDR design.

ex 1) The control signal line such as CPU is connected.

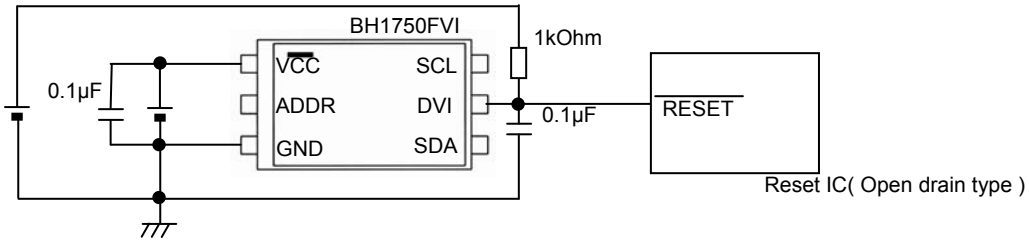


ex 2) Reset IC is used.

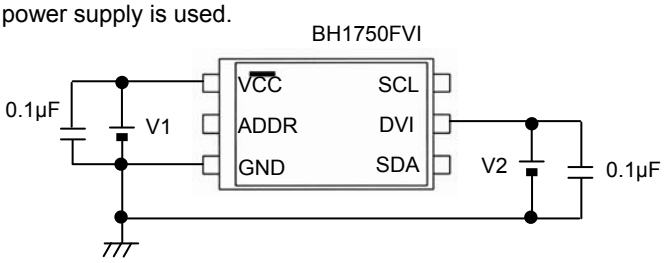
1, For Reset IC of the Push-Pull type



2, For Reset IC of the Open drain output

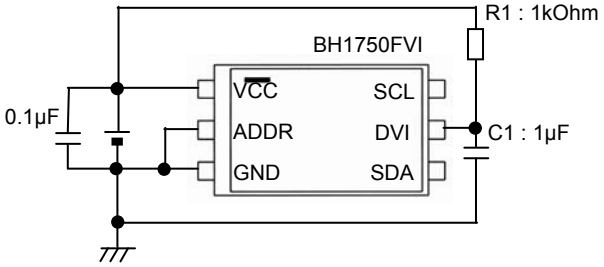


ex 3) A different power supply is used.



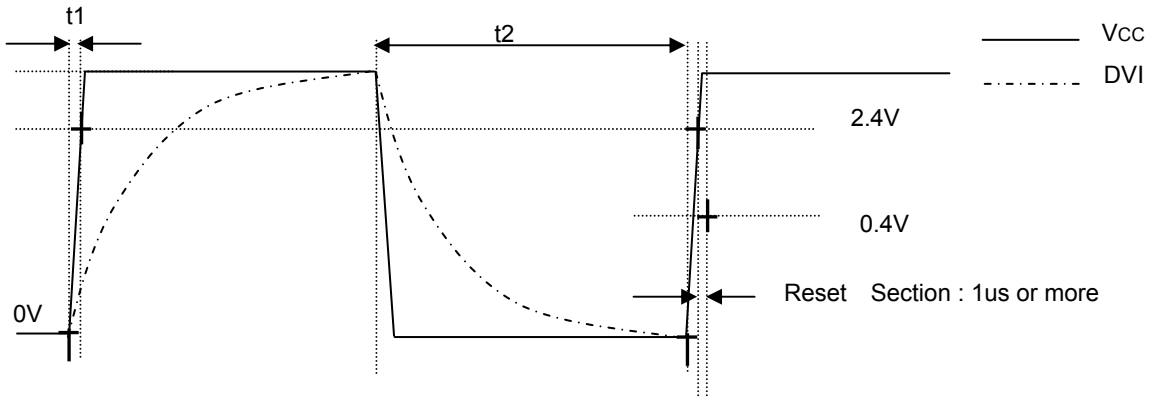
※ Power supply of DVI must stand up later than power supply of VCC stand up, because it is necessary to secure reset section (1μs or more).

ex 4) LPF using CR is inserted between VCC and DVI.
This method has the possibility that the Reset section of turning on the power supply can not satisfied. cannot be satisfied.
Please design the set considering the characteristic of the power supply enough.



◆ Notes when CR is inserted between VCC and DVI

※ Please note that there is a possibility that reset section (1μs) can not be satisfied because the power supply is turned on when the rise time of VCC is slow
※ When VCC is turned off, the DVI voltage becomes higher than VCC voltage but IC destruction is not occred if recommended constant (R1 = 1kOhm, C1 = 1μF) is used.
※ Please note that there is a possibility that Reset section (1μsec) cannot be satisfied if wait time is not enough long after turning off VCC. (It is necessary to consider DVI voltage level after turning off VCC.)

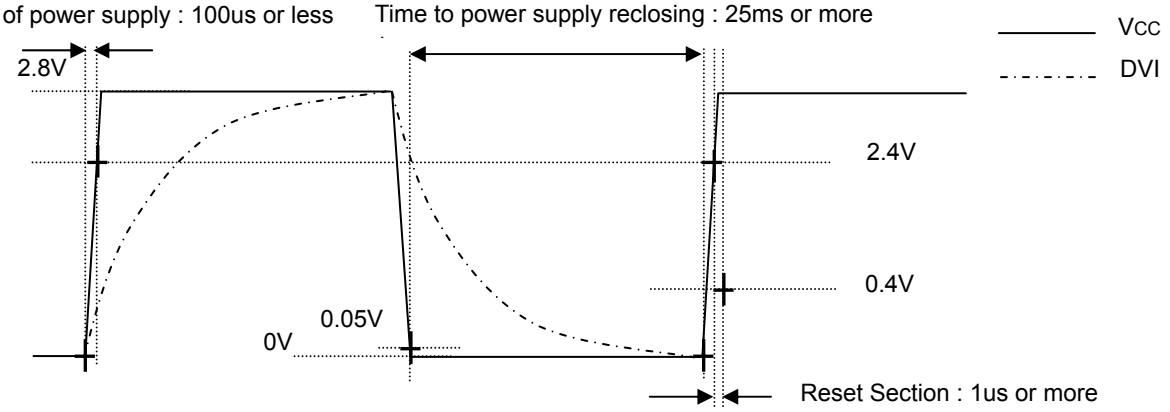


* Please do the application design to secure Reset section 1us or more after the reclosing of the power supply.

◆ Example of designing set when CR (C = 1μF, R = 1kΩ) is inserted between VCC and DVI with VCC=2.8V

①The rise time to 0→2.4V of VCC must use the power supply of 100μs or less.
②Please wait 25ms or more after VCC turn off (VCC <= 0.05V), because it is necessary to secure reset section (1μs or more).

Rise time of power supply : 100us or less Time to power supply reclosing : 25ms or more

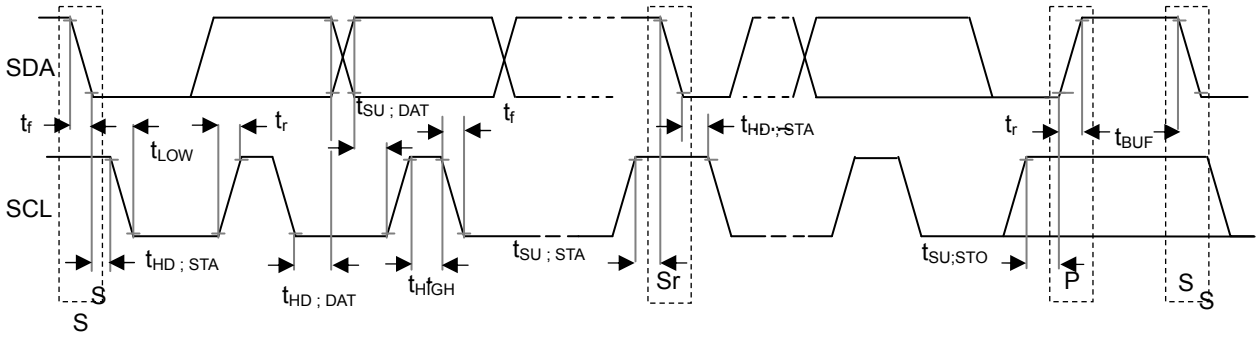


* Please do the application design to secure Reset section 1us or more after the reclosing of the power supply.

●I^2C Bus Access

1) I^2C Bus Interface Timing chart

Write measurement command and Read measurement result are done by I^2C Bus interface. Please refer the formally specification of I^2C Bus interface, and follow the formally timing chart.



2) Slave Address

Slave Address is 2 types, it is determined by ADDR Terminal

ADDR = 'H' (ADDR ≧ 0.7VCC) → "1011100"

ADDR = 'L' (ADDR ≦ 0.3VCC) → "0100011"

3) Write Format

BH1750FVI is not able to accept plural command without stop condition. Please insert SP every 1 Opecode.

ST	Slave Address	R/W 0	Ack	Opecode	Ack	SP

4) Read Format

ST	Slave Address	R/W 1	Ack	High Byte [15:8] 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 2^8	Ack

Low Byte [7:0] 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0	$\overline{Ack}$	SP

from Master to Slave

from Slave to Master

ex)

High Byte = "1000_0011"

Low Byte = "1001_0000"

($2^{15} + 2^9 + 2^8 + 2^7 + 2^4$) / 1.2 ≒ 28067 [lx]

* I^2C BUS is trademark of Phillips Semiconductors. Please refer formality specification.

●Adjust measurement result for influence of optical window. (sensor sensitivity adjusting)

BH1750FVI is possible to change sensor sensitivity. And it is possible to cancel the optical window influence (difference with / without optical window) by using this function. Adjust is done by changing measurement time. For example, when transmission rate of optical window is 50% (measurement result becomes 0.5 times if optical window is set), influence of optical window is ignored by changing sensor sensitivity from default to 2 times

Sensor sensitivity is shift by changing the value of MTreg (measurement time regisiter). MTreg value has to set 2 times if target of sensor sensitivity is 2 times. Measurement time is also set 2 times when MTreg value is changed from default to 2 times.

ex) Procedure for changing target sensor sensitivity to 2 times.

Please change Mtreg from ”0100_0101” (default) to ”1000_1010” (default * 2).

1) Changing High bit of MTreg

ST	Slave Address	R/W 0	Ack	01000_100	Ack	SP

2) Changing Low bit of MTreg

ST	Slave Address	R/W 0	Ack	011_01010	Ack	SP

3) Input Measurement Command

ST	Slave Address	R/W 0	Ack	0001_0000	Ack	SP

* This example is High Resolution mode, but it accepts the other measurement.

4) After about 240ms, measurement result is registered to Data Register.
(High Resolution mode is typically 120ms, but measurement time is set twice.)

The below table is seeing the changable range of MTreg.

		Min.	Typ.	Max.
changable range of MTreg	binary	0001_1111 (sensitivity : default * 0.45)	0100_0101 default	1111_1110 (sensitivity : default * 3.68)
	decimal	31 (sensitivity : default * 0.45)	69 default	254 (sensitivity : default * 3.68)

It is possilbe to detect 0.23lx by using this function at H-resolution mode. And it is possilbe to detect 0.11lx by using this function at H-resolution mode2.

The below formula is to calculate illuminance per 1 count.

H-reslution mode : Illuminance per 1 count (lx / count) = 1 / 1.2 *(69 / X)
H-reslution mode2 : Illuminance per 1 count (lx / count) = 1 / 1.2 *(69 / X) / 2

1.2 : Measurement accuracy
69 : Default value of MTreg (dec)
X : MTreg value

The below table is seeing the detail of resolution.

Mtreg の値	lx / count at H-resolutin mode	lx / count at H-resolution mode2
0001_1111	1.85	0.93
0100_0101	0.83	0.42
1111_1110	0.23	0.11

●H-Resolution Mode2

H-resolution mode2 is 0.5lx (typ.) resolution mode. It is suitable if under less than 10 lx measure ment data is necessary. This measurement mode supports " Adjust measurement result for influence of optical window ". Please refer it. It is possible to detect min. 0.11 lx by using H-resolution mode2.

○ Instruction set architecture for H-resolution mode2

Instruction	Opecode	Comments
Continuously H-Resolution Mode2	0001_0001	Start measurement at 0.5lx resolution. Measurement Time is typically 120ms.
One Time H-Resolution Mode2	0010_0001	Start measurement at 0.5lx resolution. Measurement Time is typically 120ms. It is automatically set to Power Down mode after measurement.

○ Measurement sequence example from "Write instruction" to "Read measurement result"

ex) Continuously H-resolution mode2 (ADDR = 'L')

from Master to Slave

from Slave to Master

① Send "Continuously H-resolution mode2 " instruction

ST	0100011	0	Ack	00010001	Ack	SP

② Wait to complete 1st H-resolution mode2 measurement.(max. 180ms.)

③ Read measurement result.

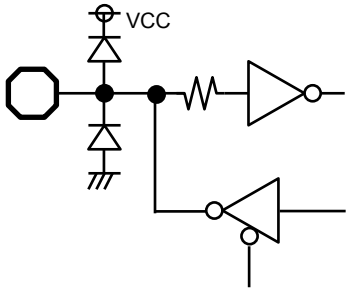
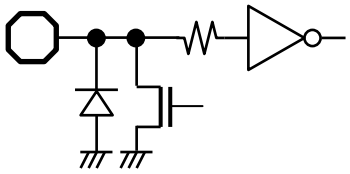
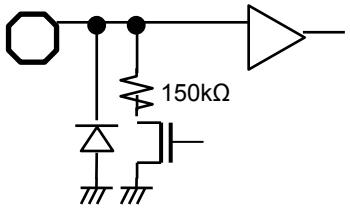
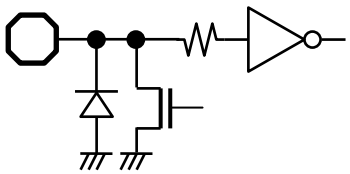
ST	0100011	1	Ack	High Byte [15:8] 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} 2^{7}	Ack

Low Byte [7:0] 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} 2^{-1}	$\overline{\text{Ack}}$	SP

How to calculate when the data High Byte is "00000000" and Low Byte is "00010010"

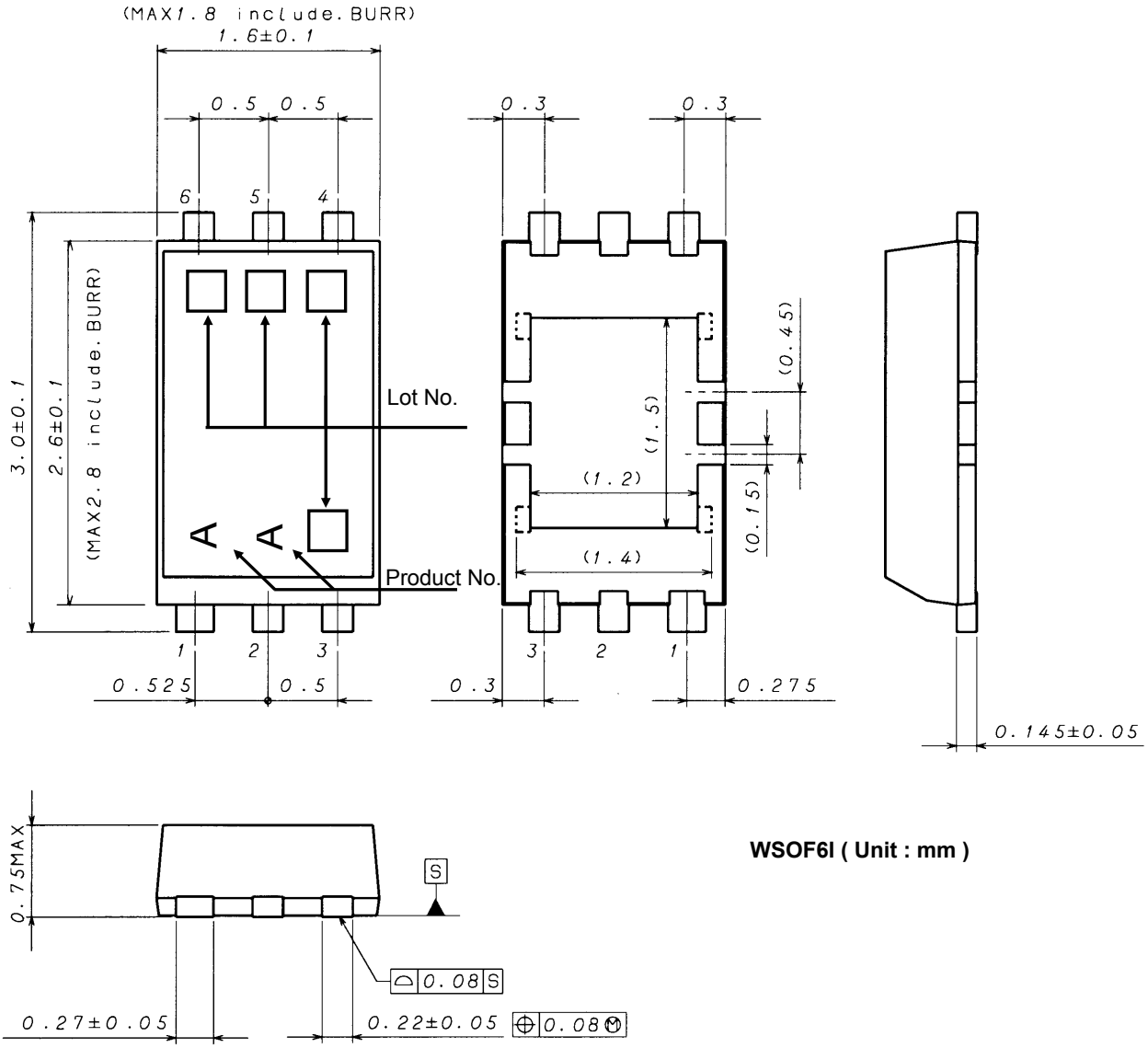
$(2^{3} + 2^{0}) / 1.2 \fallingdotseq 7.5$ [lx]

●Terminal Description

PIN No.	Terminal Name	Equivalent Circuit	Function
1	VCC		Power Supply Terminal
2	ADDR		I^2C Slave-address Terminal ADDR = 'H' (ADDR ≧ 0.7Vcc) "1011100" ADDR = 'L' (ADDR ≦ 0.3Vcc) "0100011" ADDR Terminal is designed as 3 state buffer for internal test. So that please take care of Vcc and DVI supply procedure.Please see P6.
3	GND		GND Terminal
4	SDA		I^2C bus Interface SDA Terminal
5	DVI		SDA, SCL Reference Voltage Terminal And DVI Terminal is also asynchronous Reset for internal registers.So that please set to 'L' (at least 1µs, DVI <= 0.4V) after Vcc is supplied. BH1750FVI is pulled down by 150kOhm while DVI = 'L'.
6	SCL		I^2C bus Interface SCL Terminal

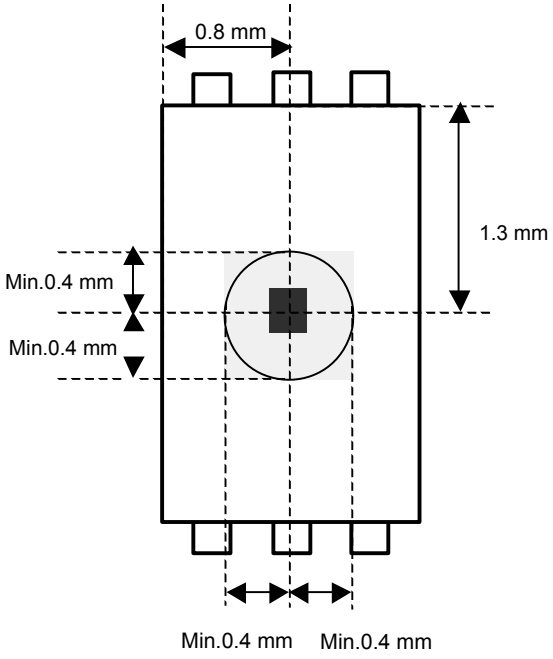
※These values are design-value, not guaranteed.

●Package Outlines



WSOF6I (Unit : mm)

●About an optical design on the device



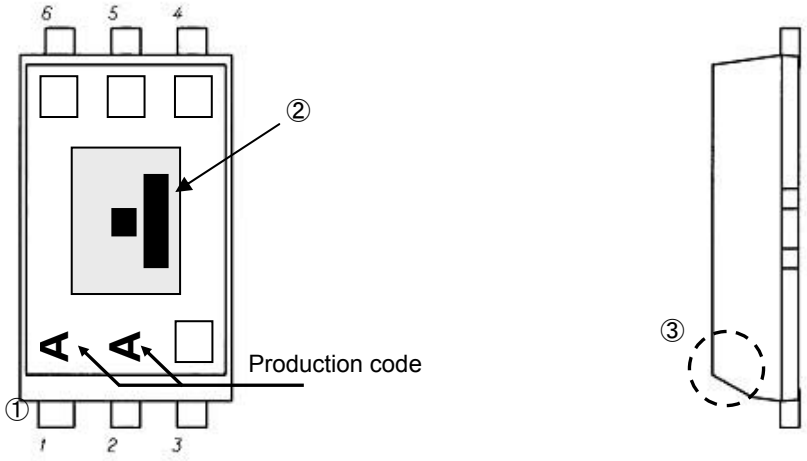
PD area (0.25 mm x 0.3 mm)

Please design the optical window so that light can cover at least this area.

●The method of distinguishing 1pin.

There is some method of distinguishing 1pin.
① Distinguishing by 1Pin wide-lead
② Distinguishing by die pattern
③ Distinguishing by taper part of 1-3pin side

② (by die patern) is the easiest method to distinguish by naked eye.



●Cautions on use

1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage (Vmax), temperature range of operating conditions (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

3) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

4) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

5) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

6) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals; such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

7) Thermal design
Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

8) Treatment of package
Dusts or scratch on the photo detector may affect the optical characteristics. Please handle it with care.

9) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

10) The exposed central pad on the back side of the package
There is an exposed central pad on the back side of the package. But please do it non connection. (Don't solder, and don't do electrical connection) Please mount by Footprint dimensions described in the Jisso Information for WSOF6I. This pad is GND level, therefore there is a possibility that LSI malfunctions and heavy-current is generated.

●Ordering part number

B	H	1	7	5	0	F	V	I	-	T	R

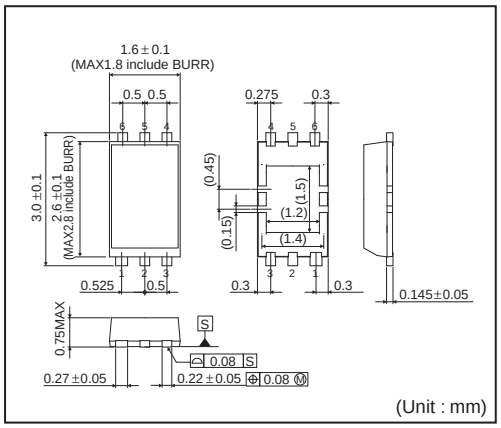
Part No. (BH)

Part No. (1750)

Package
FVI: WSOF6I

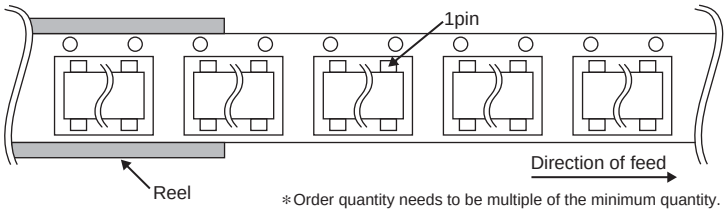
Packaging and forming specification
TR: Embossed tape and reel

WSOF6I



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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http://www.rohm.com/contact/

3500/32M 4-Channel Relay Module

Datasheet

Bently Nevada Machinery Condition Monitoring

141533 Rev. U

Description

The 4-Channel Relay Module is a full-height module that provides four relay outputs. Any number of 4-Channel Relay Modules can be placed in any of the slots to the right of the Transient Data Interface Module. Each output of the 4-Channel Relay Module can be independently programmed to perform voting logic.

Each relay utilized on the 4-Channel Relay Module includes Alarm Drive Logic.

Programming for the Alarm Drive Logic uses AND and OR logic, and can use alarming inputs (Alert and Danger statuses), Not- OK, or individual PPLs from any monitor channel or any combination of monitor channels in the rack. You can program this Alarm Drive to meet your application needs using the 3500 Rack Configuration Software.

Bently Nevada
a Baker Hughes business

Specifications

Inputs	
Power Consumption	5.8 watts typical
Outputs	
OK LED	Illuminated when module is functioning properly.
TX/RX LED	Transmit and Receive. Flashes to indicate proper communications between this module and other modules within the rack.
CH ALARM LED	Illuminated to indicate that the Relay Channel is in an alarm state.
Relays	
Type	Single-pole, double-throw (SPDT) relays
Environmental Sealing	Epoxy-sealed
Arc Suppressor	250 Vrms, installed as standard
Contact Life	100,000 cycles @ 5 A, 24 Vdc or 240 Vac
Operation	Each relay of the four channels is switch selectable for Normally De-energized or Normally Energized.

Environmental Limits

Operating Temperature	-30°C to +65°C (-22°F to +150°F)
Storage Temperature	-40°C to +85°C (-40°F to +185°F)
Humidity	95%, non-condensing

Physical Characteristics

Main Module

Dimensions (Height x Width x Depth)	241 mm x 24.4 mm x 242 mm (9.50 in. x 0.96 in. x 9.52 in.)
Weight	0.7 kg (1.6 lb.)

I/O Module

Dimensions (Height x Width x Depth)	241 mm x 24.4 mm x 99.1 mm (9.50 in. x 0.96 in. x 3.90 in.).
Weight	0.4 kg (1.0 lb.)

Rack Space Requirements

Main Module	1 full-height front slot.
I/O Modules	1 full-height rear slot.

Contact Ratings for Standard Systems

Standard Relays

Minimum switched current	100 mA @ 12 Vdc
DC specifications (Resistive load)	
Maximum switched current	2 A @ 0V to 30 Vdc 0.75 A @ 48 Vdc 0.2 A @ 125 Vdc
Max switched voltage	125 Vdc
AC specifications (Resistive load)	
Maximum switched voltage	250 Vac
Maximum switched current	2 A
Maximum switched power	450 VA

Contact Ratings For Functional Safety Systems and Hazardous Area Systems

Standard Relays

Minimum switched current	100 mA @ 12 Vdc
DC specifications (Resistive load)	
Maximum switched current	2 A @ 0V to 30 Vdc
Maximum switched voltage	30 Vdc
AC specifications (Resistive Load)	
Maximum Switched Voltage	30 Vac
Maximum Switched Current	2 A

WARNING

Due to the potential for varying voltage levels, please review the following:

- 3500 monitors ordered with hazardous approvals options (01 & -02) are certified to Division 2/Zone 2 standards (including ATEX/IECEx and North American Zones and Divisions). The Division 2 /Zone 2 standards specify increased spacing requirements at higher voltages, and the 3500/32M relays **do not** meet these spacing requirements. For this reason, 3500/32M relays ordered with the hazardous area approvals options (including country-specific hazardous area approvals options) have historically been limited to a lower voltage than those ordered with non-hazardous approvals options. Using higher voltages would violate the hazardous area certificates associated with the hazardous area approvals option.
- If the 3500/32M is part of a functional safety (SIL) system, the functional safety certificate requires the restricted voltage. Higher voltages are not allowed for functional safety (SIL) systems.
- It is possible to connect field wiring to the 3500/32M relays such that conductors are exposed to potential human contact. This could present a shock hazard at high voltages. Customers shall only use the 3500/32M relays at the voltages specified. Appropriate safety precautions must be taken with respect to the shock hazard.

Compliance and Certifications (Approvals Pending)

FCC

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

EMC

European Community Directive:

EMC Directive 2014/30/EU

Standards:

EN 61000-6-2; Immunity for Industrial Environments
EN 61000-6-4; Emissions for Industrial Environments

Electrical Safety

European Community Directive:

LV Directive 2014/35/EU

Standards:

EN 61010-1

RoHS

European Community Directive:

RoHS Directive 2011/65/EU

Cyber Security

Designed to meet IEC 62443

Maritime

DNV GL rules for classification – Ships, offshore units, and high speed and light craft

ABS Rules for Condition of Classification, Part 1

- Steel Vessels Rules
- Offshore Units and Structures

Functional Safety

SIL 2

Hazardous Area Approvals

For the detailed listing of country and product specific approvals, refer to the *Approvals Quick Reference Guide* (108M1756) available from Bently.com.

cNRTLus

Class I, Zone 2: AEx/Ex nA nC ic IIC T4 Gc;
Class I, Zone 2: AEx/Ex ec nC ic IIC T4 Gc;
Class I, Division 2, Groups A, B, C, and D;

T4 @ Ta= -20˚C to +65˚C (-4˚F to +149˚F)
When installed per drawing 149243 or 149244.

ATEX/IECEx

II 3 G

Ex nA nC ic IIC T4 Gc
Ex ec nC ic IIC T4 Gc

T4 @ Ta= -20˚C to +65˚C
(-4˚F to +149˚F)
When installed per drawing 149243 or 149244.

Ordering Considerations

Firmware, Software, and Hardware Requirements

The 3500/32M requires the 3500/22 Transient Data Interface (TDI) module. It also requires these or newer versions of the following firmware and software:

3500/32M Firmware	N.NN, Rev. X
3500/22 Firmware (TDI)	Rev 1.71
3500/01 Software (Rack Config)	Rev 4.5
3500/02 Software (Op Display)	Rev 2.21
3500/03 Software (Data Acquisition)	Rev 2.4
3500/94 VGA display	Rev C
3500/93 LCD display	Rev P

- The 3500/32M requires 3500 Rack Configuration software, version 4.5 or later.
- The 3500/32M requires 3500 Data Acquisition software, version 2.40 or later.
- The 3500/32M requires 3500 Data Display software, version 1.40 or later.
- When used with a 3500/93 LCD Display module, the 3500/93 will require firmware revision P or later.
- When used with a 3500/94 VGA Display module, the 3500/94 will require firmware revision C or later.

Ordering Information

For the detailed listing of country and product specific approvals, refer to the *Approvals Quick Reference Guide* (108M1756) available from Bently.com.

3500 4-Channel Relay Module

3500/32 -AA-BB

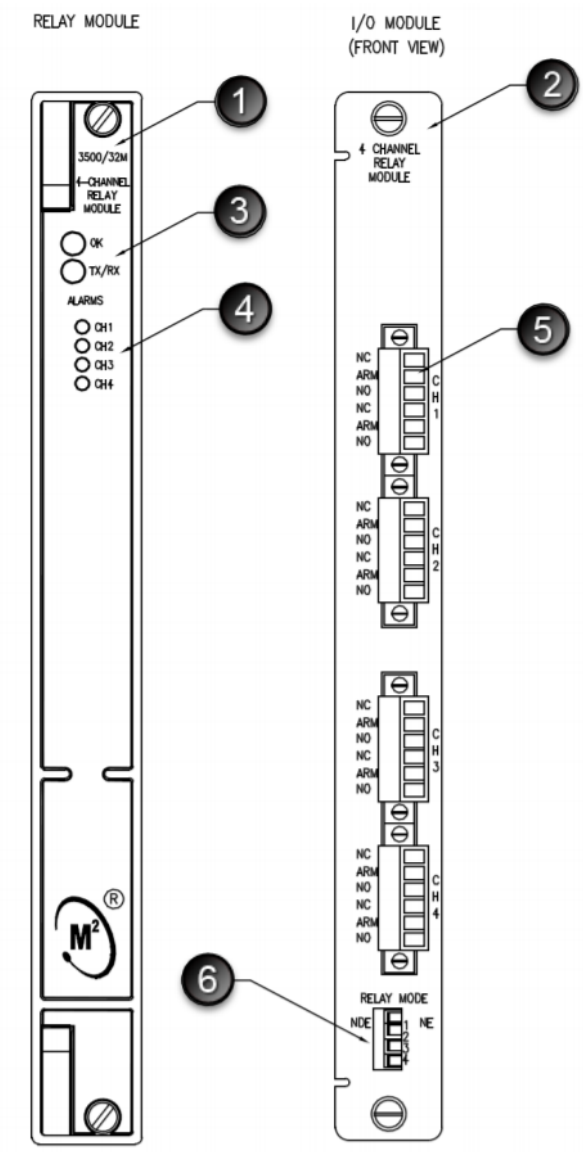
A: Output Module	
01	4-Channel Relay Output Module
B: Agency Approval Option	
00	None
01	cNRTLus (Class I, Div 2)
02	ATEX/IECEx/CSA (Class I, Zone 2)

Spares

149986-02	Spare 4-Channel Relay Control Module
125720-01	Spare 4-Channel Relay Output Module (available for repair only)
125720-02	Spare 4-Channel Relay Output Module for hazardous area systems and functional safety systems
04425545	Grounding wrist strap (single use)
00580453	Connector header, internal termination, 16-position, green
00580436	Connector header, internal termination, 6-position, green
166M2390	Connector header, push-in-spring type (alternative for PN 00580436)

For more information, please refer to the 3500/32 and 3500/32M 4-Channel and 3500/34 TMR Relay Modules User Guide (document 129771).

Graphs and Figures



1. Relay module
2. I/O module
3. Status LEDs
4. Relay channel LEDs
5. Relay contacts
6. Relay mode selection switch

Figure 1: Front and Rear View of the 4-Channel Relay Module

1631 Bently Parkway South, Minden, Nevada USA 89423
Phone: 1.775.782.3611 (US) or Bently.com/support
Bently.com

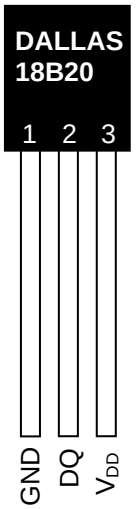
DS18B20
Programmable Resolution 1-Wire Digital Thermometer

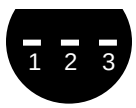
www.maxim-ic.com

FEATURES

- Unique 1-Wire® interface requires only one port pin for communication
- Each device has a unique 64-bit serial code stored in an onboard ROM
- Multidrop capability simplifies distributed temperature sensing applications
- Requires no external components
- Can be powered from data line. Power supply range is 3.0V to 5.5V
- Measures temperatures from –55°C to +125°C (–67°F to +257°F)
- ±0.5°C accuracy from –10°C to +85°C
- Thermometer resolution is user-selectable from 9 to 12 bits
- Converts temperature to 12-bit digital word in 750ms (max.)
- User-definable nonvolatile (NV) alarm settings
- Alarm search command identifies and addresses devices whose temperature is outside of programmed limits (temperature alarm condition)
- Available in 8-pin SO (150mil), 8-pin µSOP, and 3-pin TO-92 packages
- Software compatible with the DS1822
- Applications include thermostatic controls, industrial systems, consumer products, thermometers, or any thermally sensitive system

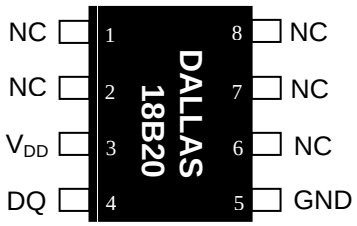
PIN ASSIGNMENT



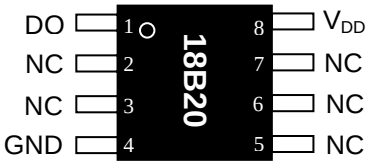


(BOTTOM VIEW)

TO-92
(DS18B20)



8-Pin 150mil SO
(DS18B20Z)



8-Pin µSOP
(DS18B20U)

PIN DESCRIPTION

GND - Ground
DQ - Data In/Out
V_{DD} - Power Supply Voltage
NC - No Connect

DESCRIPTION

The DS18B20 Digital Thermometer provides 9 to 12–bit centigrade temperature measurements and has an alarm function with nonvolatile user-programmable upper and lower trigger points. The DS18B20 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. It has an operating temperature range of –55°C to +125°C and is accurate to ±0.5°C over the range of –10°C to +85°C. In addition, the DS18B20 can derive power directly from the data line (“parasite power”), eliminating the need for an external power supply.

Each DS18B20 has a unique 64-bit serial code, which allows multiple DS18B20s to function on the same 1–wire bus; thus, it is simple to use one microprocessor to control many DS18B20s distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment or machinery, and process monitoring and control systems.

1-Wire is a registered trademark of Dallas Semiconductor.

ORDER INFORMATION

ORDERING NUMBER	PACKAGE MARKING	DESCRIPTION
DS18B20	18B20	DS18B20 in 3-pin TO92
DS18B20/T&R	18B20	DS18B20 in 3-pin TO92, 2000 Piece Tape-and-Reel
DS18B20+	18B20 (See Note)	DS18B20 in Lead-Free 3-pin TO92
DS18B20+T&R	18B20 (See Note)	DS18B20 in Lead-Free 3-pin TO92, 2000 Piece Tape-and-Reel
DS18B20U	18B20	DS18B20 in 8-pin uSOP
DS18B20U/T&R	18B20	DS18B20 in 8-pin uSOP, 3000 Piece Tape-and-Reel
DS18B20U+	18B20 (See Note)	DS18B20 in Lead-Free 8-pin uSOP
DS18B20U+T&R	18B20 (See Note)	DS18B20 in Lead-Free 8-pin uSOP, 3000 Piece Tape-and-Reel
DS18B20Z	DS18B20	DS18B20 in 150 mil 8-pin SO
DS18B20Z/T&R	DS18B20	DS18B20 in 150 mil 8-pin SO, 2500 Piece Tape-and-Reel
DS18B20Z+	DS18B20 (See Note)	DS18B20 in Lead-Free 150 mil 8-pin SO
DS18B20Z+T&R	DS18B20 (See Note)	DS18B20 in Lead-Free 150 mil 8-pin SO, 2500 Piece Tape-and-Reel

Note: A "+" symbol will also be marked on the package.

DETAILED PIN DESCRIPTIONS Table 1

SO*	μSOP*	TO-92	SYMBOL	DESCRIPTION
5	4	1	GND	**Ground.**
4	1	2	DQ	**Data Input/Output pin.** Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode (see "Parasite Power" section.)
3	8	3	V_{DD}	**Optional V_{DD} pin.** V_{DD} must be grounded for operation in parasite power mode.

*All pins not specified in this table are "No Connect" pins.

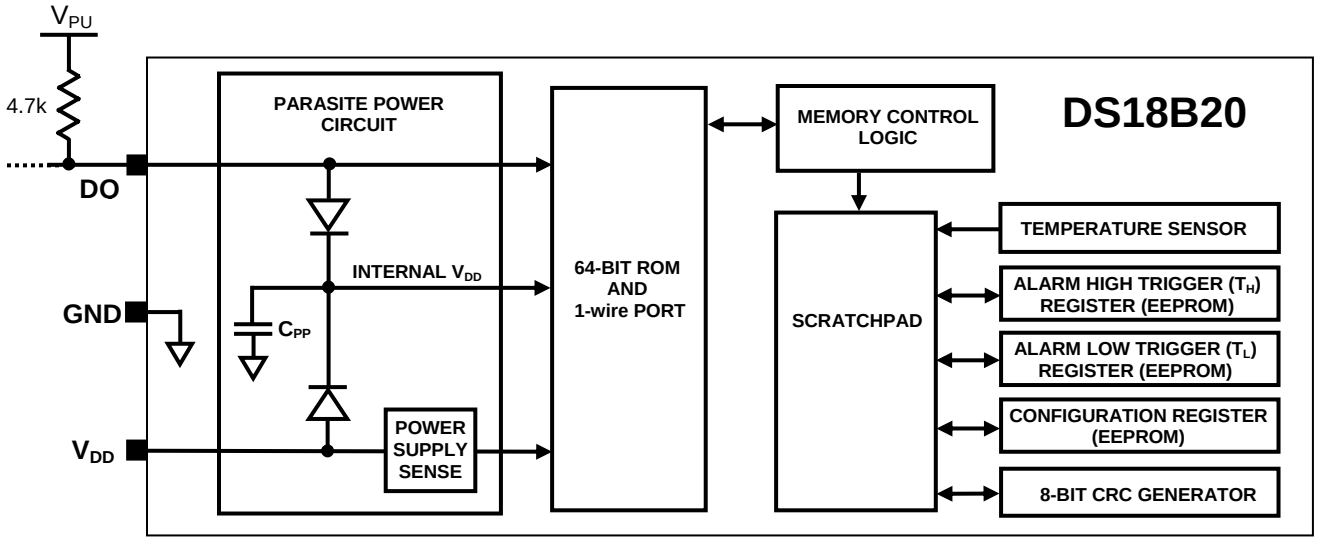
OVERVIEW

Figure 1 shows a block diagram of the DS18B20, and pin descriptions are given in Table 1. The 64-bit ROM stores the device's unique serial code. The scratchpad memory contains the 2-byte temperature register that stores the digital output from the temperature sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (T_H and T_L), and the 1-byte configuration register. The configuration register allows the user to set the resolution of the temperature-to-digital conversion to 9, 10, 11, or 12 bits. The T_H, T_L and configuration registers are nonvolatile (EEPROM), so they will retain data when the device is powered down.

The DS18B20 uses Dallas' exclusive 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the DS18B20). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device's unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and "time slots," is covered in the *1-WIRE BUS SYSTEM* section of this datasheet.

Another feature of the DS18B20 is the ability to operate without an external power supply. Power is instead supplied through the 1-Wire pullup resistor via the DQ pin when the bus is high. The high bus signal also charges an internal capacitor (C_{PP}), which then supplies power to the device when the bus is low. This method of deriving power from the 1-Wire bus is referred to as "parasite power." As an alternative, the DS18B20 may also be powered by an external supply on V_{DD}.

DS18B20 BLOCK DIAGRAM Figure 1



OPERATION — MEASURING TEMPERATURE

The core functionality of the DS18B20 is its direct-to-digital temperature sensor. The resolution of the temperature sensor is user-configurable to 9, 10, 11, or 12 bits, corresponding to increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The default resolution at power-up is 12-bit. The DS18B20 powers-up in a low-power idle state; to initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18B20 returns to its idle state. If the DS18B20 is powered by an external supply, the master can issue "read time slots" (see the *1-WIRE BUS SYSTEM* section) after the Convert T command and the DS18B20 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. If the DS18B20 is powered with parasite power, this notification technique cannot be used since the bus must be pulled high by a strong pullup during the entire temperature conversion. The bus requirements for parasite power are explained in detail in the *POWERING THE DS18B20* section of this datasheet.

The DS18B20 output temperature data is calibrated in degrees centigrade; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two's complement number in the temperature register (see Figure 2). The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. If the DS18B20 is configured for 12-bit resolution, all bits in the temperature register will contain valid data. For 11-bit resolution, bit 0 is undefined. For 10-bit resolution, bits 1 and 0 are undefined, and for 9-bit resolution bits 2, 1 and 0 are undefined. Table 2 gives examples of digital output data and the corresponding temperature reading for 12-bit resolution conversions.

TEMPERATURE REGISTER FORMAT Figure 2

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LS Byte	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
	bit 15	**bit 14**	**bit 13**	**bit 12**	**bit 11**	**bit 10**	**bit 9**	**bit 8**
MS Byte	S	S	S	S	S	2^6	2^5	2^4

TEMPERATURE/DATA RELATIONSHIP Table 2

TEMPERATURE	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0000 0111 1101 0000	07D0h
+85°C*	0000 0101 0101 0000	0550h
+25.0625°C	0000 0001 1001 0001	0191h
+10.125°C	0000 0000 1010 0010	00A2h
+0.5°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
-0.5°C	1111 1111 1111 1000	FFF8h
-10.125°C	1111 1111 0101 1110	FF5Eh
-25.0625°C	1111 1110 0110 1111	FE6Fh
-55°C	1111 1100 1001 0000	FC90h

*The power-on reset value of the temperature register is +85°C

OPERATION — ALARM SIGNALING

After the DS18B20 performs a temperature conversion, the temperature value is compared to the user-defined two's complement alarm trigger values stored in the 1-byte T_H and T_L registers (see Figure 3). The sign bit (S) indicates if the value is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The T_H and T_L registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. T_H and T_L can be accessed through bytes 2 and 3 of the scratchpad as explained in the *MEMORY* section of this datasheet.

T_H AND T_L REGISTER FORMAT Figure 3

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
S	2^6	2^5	2^5	2^5	2^2	2^1	2^0

Only bits 11 through 4 of the temperature register are used in the T_H and T_L comparison since T_H and T_L are 8-bit registers. If the measured temperature is lower than or equal to T_L or higher than or equal to T_H, an alarm condition exists and an alarm flag is set inside the DS18B20. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion.

The master device can check the alarm flag status of all DS18B20s on the bus by issuing an Alarm Search [ECh] command. Any DS18B20s with a set alarm flag will respond to the command, so the master can determine exactly which DS18B20s have experienced an alarm condition. If an alarm condition exists and the T_H or T_L settings have changed, another temperature conversion should be done to validate the alarm condition.

POWERING THE DS18B20

The DS18B20 can be powered by an external supply on the V_{DD} pin, or it can operate in "parasite power" mode, which allows the DS18B20 to function without a local external supply. Parasite power is very useful for applications that require remote temperature sensing or that are very space constrained. Figure 1 shows the DS18B20's parasite-power control circuitry, which "steals" power from the 1-Wire bus via the DQ pin when the bus is high. The stolen charge powers the DS18B20 while the bus is high, and some of the charge is stored on the parasite power capacitor (C_{PP}) to provide power when the bus is low. When the DS18B20 is used in parasite power mode, the V_{DD} pin must be connected to ground.

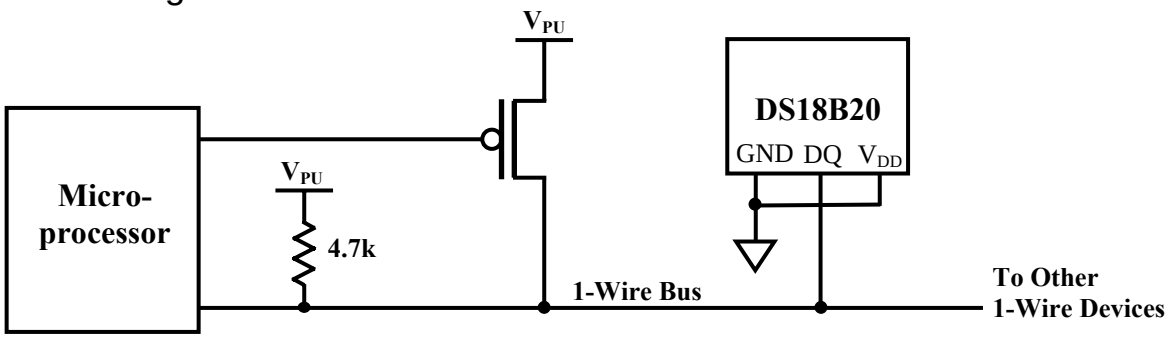
In parasite power mode, the 1-Wire bus and C_{PP} can provide sufficient current to the DS18B20 for most operations as long as the specified timing and voltage requirements are met (refer to *the DC ELECTRICAL CHARACTERISTICS* and the *AC ELECTRICAL CHARACTERISTICS* sections of this data sheet). However, when the DS18B20 is performing temperature conversions or copying data from the scratchpad memory to EEPROM, the operating current can be as high as 1.5mA. This current can cause an unacceptable voltage drop across the weak 1-Wire pullup resistor and is more current than can be supplied by C_{PP}. To assure that the DS18B20 has sufficient supply current, it is necessary to provide a strong pullup on the 1-Wire bus whenever temperature conversions are taking place or data is being copied from the scratchpad to EEPROM. This can be accomplished by using a MOSFET to pull the bus directly to the rail as shown in Figure 4. The 1-Wire bus must be switched to the strong pullup within 10µs (max) after a Convert T [44h] or Copy Scratchpad [48h] command is issued, and the bus must be held high by the pullup for the duration of the conversion (t_{conv}) or data transfer (t_{wr} = 10ms). No other activity can take place on the 1-Wire bus while the pullup is enabled.

The DS18B20 can also be powered by the conventional method of connecting an external power supply to the V_{DD} pin, as shown in Figure 5. The advantage of this method is that the MOSFET pullup is not required, and the 1-Wire bus is free to carry other traffic during the temperature conversion time.

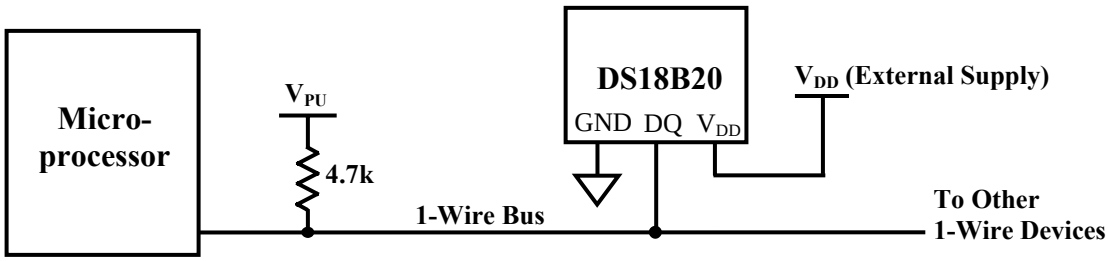
The use of parasite power is not recommended for temperatures above +100°C since the DS18B20 may not be able to sustain communications due to the higher leakage currents that can exist at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that the DS18B20 be powered by an external power supply.

In some situations the bus master may not know whether the DS18B20s on the bus are parasite powered or powered by external supplies. The master needs this information to determine if the strong bus pullup should be used during temperature conversions. To get this information, the master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a "read time slot". During the read time slot, parasite powered DS18B20s will pull the bus low, and externally powered DS18B20s will let the bus remain high. If the bus is pulled low, the master knows that it must supply the strong pullup on the 1-Wire bus during temperature conversions.

SUPPLYING THE PARASITE-POWERED DS18B20 DURING TEMPERATURE CONVERSIONS Figure 4



POWERING THE DS18B20 WITH AN EXTERNAL SUPPLY Figure 5



64-BIT LASERED ROM CODE

Each DS18B20 contains a unique 64–bit code (see Figure 6) stored in ROM. The least significant 8 bits of the ROM code contain the DS18B20's 1-Wire family code: 28h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. A detailed explanation of the CRC bits is provided in the *CRC GENERATION* section. The 64-bit ROM code and associated ROM function control logic allow the DS18B20 to operate as a 1-Wire device using the protocol detailed in the *1-WIRE BUS SYSTEM* section of this datasheet.

64-BIT LASERED ROM CODE Figure 6

8-BIT CRC		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE (28h)	
MSB	LSB	MSB	LSB	MSB	LSB

MEMORY

The DS18B20's memory is organized as shown in Figure 7. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (T_H and T_L) and configuration register. Note that if the DS18B20 alarm function is not used, the T_H and T_L registers can serve as general-purpose memory. All memory commands are described in detail in the *DS18B20 FUNCTION COMMANDS* section.

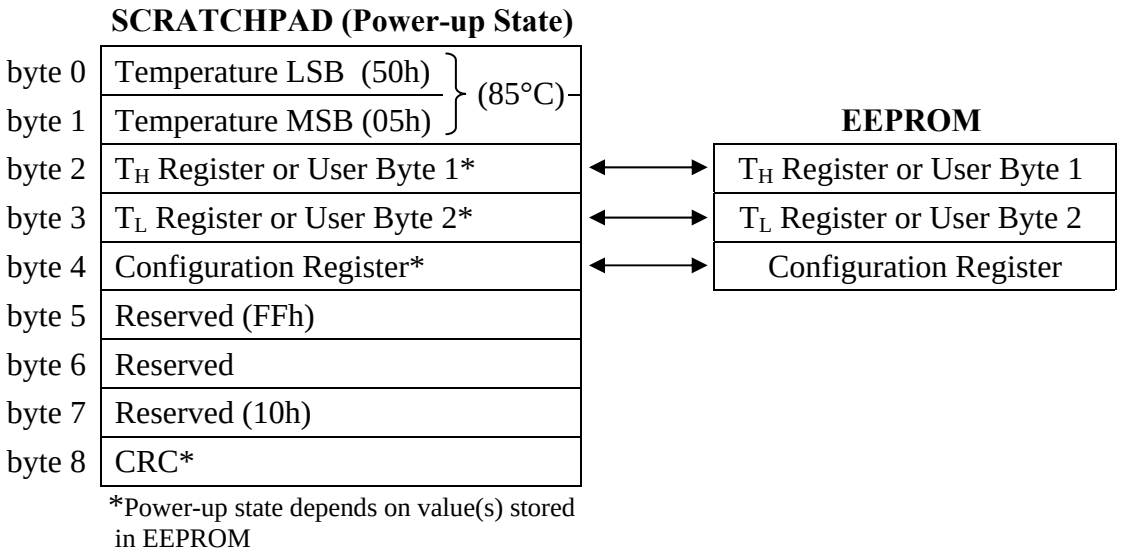
Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to T_H and T_L registers. Byte 4 contains the configuration register data, which is explained in detail in the CONFIGURATION REGISTER section of this datasheet. Bytes 5, 6, and 7 are reserved for internal use by the device and cannot be overwritten.

Byte 8 of the scratchpad is read-only and contains the cyclic redundancy check (CRC) code for bytes 0 through 7 of the scratchpad. The DS18B20 generates this CRC using the method described in *the CRC GENERATION* section.

Data is written to bytes 2, 3, and 4 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the DS18B20 starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the T_H, T_L and configuration data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command.

Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratchpad at any time using the Recall E^2 [B8h] command. The master can issue read time slots following the Recall E^2 command and the DS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done.

DS18B20 MEMORY MAP Figure 7



*Power-up state depends on value(s) stored in EEPROM

CONFIGURATION REGISTER

Byte 4 of the scratchpad memory contains the configuration register, which is organized as illustrated in Figure 8. The user can set the conversion resolution of the DS18B20 using the R0 and R1 bits in this register as shown in Table 3. The power-up default of these bits is R0 = 1 and R1 = 1 (12-bit resolution). Note that there is a direct tradeoff between resolution and conversion time. Bit 7 and bits 0 to 4 in the configuration register are reserved for internal use by the device and cannot be overwritten.

CONFIGURATION REGISTER Figure 8

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	R1	R0	1	1	1	1	1

THERMOMETER RESOLUTION CONFIGURATION Table 3

R1	R0	Resolution	Max Conversion Time	
0	0	9-bit	93.75 ms	($t_{CONV}/8$)
0	1	10-bit	187.5 ms	($t_{CONV}/4$)
1	0	11-bit	375 ms	($t_{CONV}/2$)
1	1	12-bit	750 ms	(t_{CONV})

CRC GENERATION

CRC bytes are provided as part of the DS18B20's 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The scratchpad CRC is calculated from the data stored in the scratchpad, and therefore it changes when the data in the scratchpad changes. The CRCs provide the bus master with a method of data validation when data is read from the DS18B20. To verify that data has been read correctly, the bus master must re-calculate the CRC from the received data and then compare this value to either the ROM code CRC (for ROM reads) or to the scratchpad CRC (for scratchpad reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS18B20 that prevents a command sequence from proceeding if the DS18B20 CRC (ROM or scratchpad) does not match the value generated by the bus master.

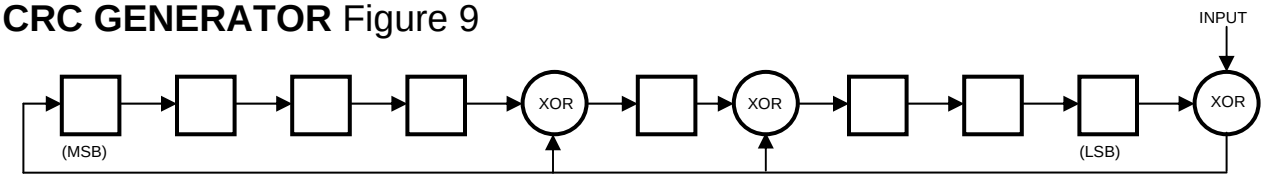
The equivalent polynomial function of the CRC (ROM or scratchpad) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus master can re-calculate the CRC and compare it to the CRC values from the DS18B20 using the polynomial generator shown in Figure 9. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code or the least significant bit of byte 0 in the scratchpad, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the scratchpad, the polynomial generator will contain the re-calculated CRC. Next, the 8-bit ROM code or scratchpad CRC from the DS18B20 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s. Additional information about the Dallas 1-Wire cyclic redundancy check

is available in *Application Note 27: Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products*.

CRC GENERATOR Figure 9



1-WIRE BUS SYSTEM

The 1-Wire bus system uses a single bus master to control one or more slave devices. The DS18B20 is always a slave. When there is only one slave on the bus, the system is referred to as a "single-drop" system; the system is "multidrop" if there are multiple slaves on the bus.

All data and commands are transmitted least significant bit first over the 1-Wire bus.

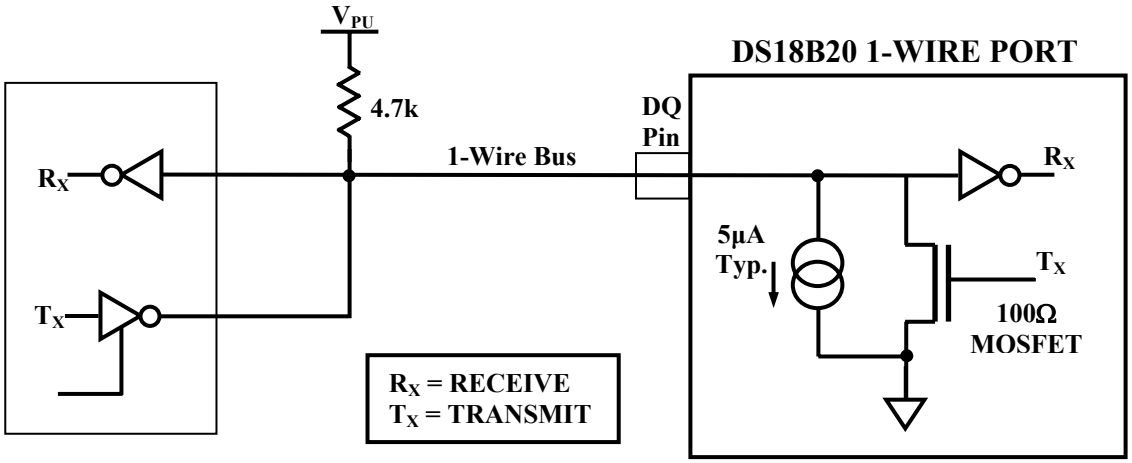
The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open-drain or 3-state port. This allows each device to "release" the data line when the device is not transmitting data so the bus is available for use by another device. The 1-Wire port of the DS18B20 (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 10.

The 1-Wire bus requires an external pullup resistor of approximately 5kΩ; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 480µs, all components on the bus will be reset.

HARDWARE CONFIGURATION Figure 10



TRANSACTION SEQUENCE

The transaction sequence for accessing the DS18B20 is as follows:

Step 1. Initialization

Step 2. ROM Command (followed by any required data exchange)

Step 3. DS18B20 Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the DS18B20 is accessed, as the DS18B20 will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM [F0h] and Alarm Search [ECh] commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the DS18B20) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the *1-WIRE SIGNALING* section.

ROM COMMANDS

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a DS18B20 function command. A flowchart for operation of the ROM commands is shown in Figure 11.

SEARCH ROM [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM command (see below) can be used in place of the Search ROM process. For a detailed explanation of the Search ROM procedure, refer to the *iButton® Book of Standards* at www.ibutton.com/ibuttons/standard.pdf. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

READ ROM [33h]

This command can only be used when there is one slave on the bus. It allows the bus master to read the slave's 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

MATCH ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multidrop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

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SKIP ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all DS18B20s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case time is saved by allowing the master to read from the slave without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

ALARM SEARCH [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if any DS18B20s experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must return to Step 1 (Initialization) in the transaction sequence. Refer to the *OPERATION — ALARM SIGNALING* section for an explanation of alarm flag operation.

DS18B20 FUNCTION COMMANDS

After the bus master has used a ROM command to address the DS18B20 with which it wishes to communicate, the master can issue one of the DS18B20 function commands. These commands allow the master to write to and read from the DS18B20's scratchpad memory, initiate temperature conversions and determine the power supply mode. The DS18B20 function commands, which are described below, are summarized in Table 4 and illustrated by the flowchart in Figure 12.

CONVERT T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18B20 returns to its low-power idle state. If the device is being used in parasite power mode, within 10μs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for the duration of the conversion (t_{conv}) as described in the *POWERING THE DS18B20* section. If the DS18B20 is powered by an external supply, the master can issue read time slots after the Convert T command and the DS18B20 will respond by transmitting a 0 while the temperature conversion is in progress and a 1 when the conversion is done. In parasite power mode this notification technique cannot be used since the bus is pulled high by the strong pullup during the conversion.

WRITE SCRATCHPAD [4Eh]

This command allows the master to write 3 bytes of data to the DS18B20's scratchpad. The first data byte is written into the T_H register (byte 2 of the scratchpad), the second byte is written into the T_L register (byte 3), and the third byte is written into the configuration register (byte 4). Data must be transmitted least significant bit first. All three bytes MUST be written before the master issues a reset, or the data may be corrupted.

READ SCRATCHPAD [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9^{th} byte (byte 8 – CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

COPY SCRATCHPAD [48h]

This command copies the contents of the scratchpad T_H, T_L and configuration registers (bytes 2, 3 and 4) to EEPROM. If the device is being used in parasite power mode, within 10μs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for at least 10ms as described in the *POWERING THE DS18B20* section.

RECALL E^2 [B8h]

This command recalls the alarm trigger values (T_H and T_L) and configuration data from EEPROM and places the data in bytes 2, 3, and 4, respectively, in the scratchpad memory. The master device can issue read time slots following the Recall E^2 command and the DS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

READ POWER SUPPLY [B4h]

The master device issues this command followed by a read time slot to determine if any DS18B20s on the bus are using parasite power. During the read time slot, parasite powered DS18B20s will pull the bus low, and externally powered DS18B20s will let the bus remain high. Refer to the *POWERING THE DS18B20* section for usage information for this command.

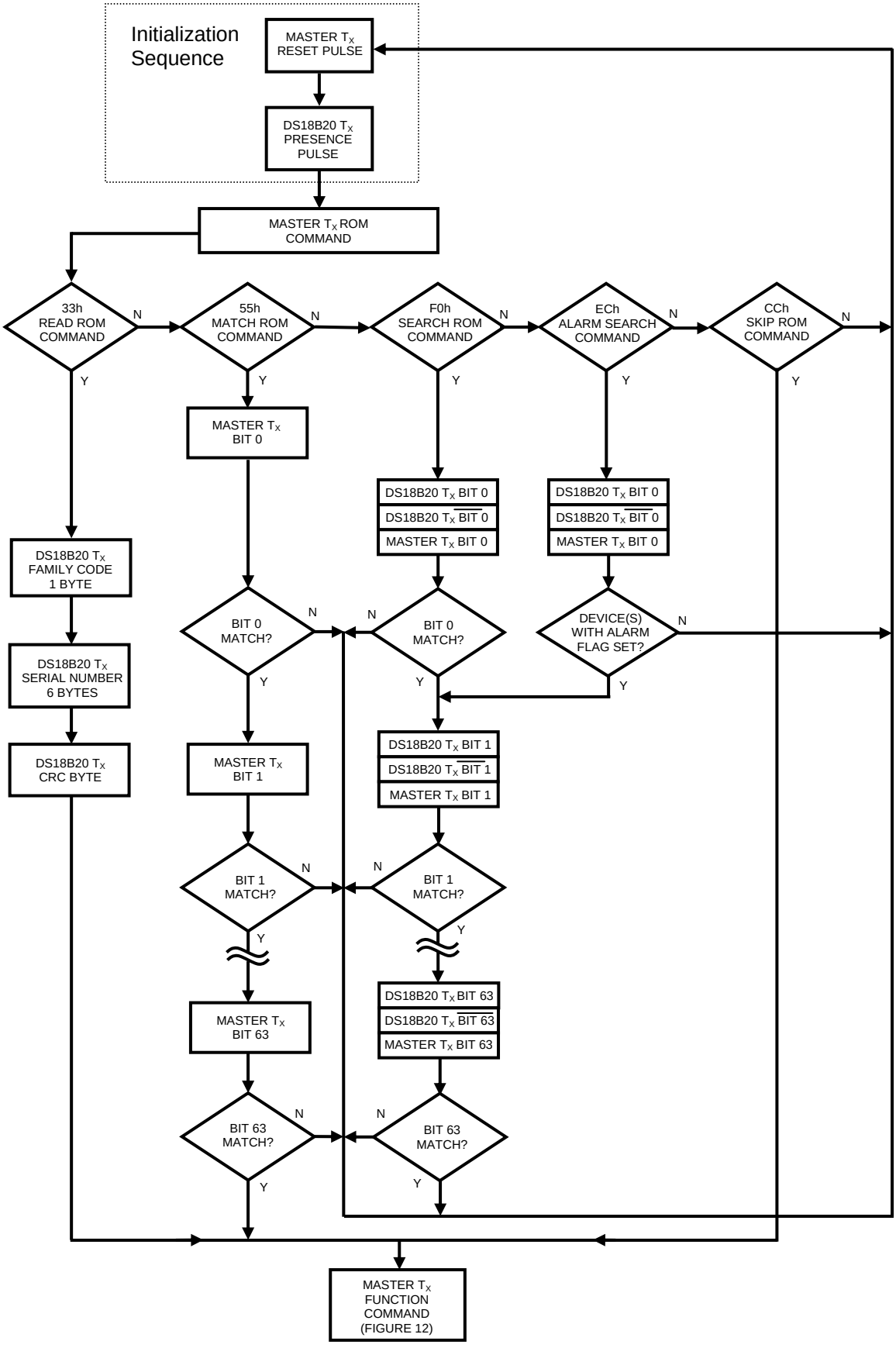
DS18B20 FUNCTION COMMAND SET Table 4

Command	Description	Protocol	1-Wire Bus Activity After Command is Issued	Notes
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	DS18B20 transmits conversion status to master (not applicable for parasite-powered DS18B20s).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	DS18B20 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, and 4 (T_H, T_L, and configuration registers).	4Eh	Master transmits 3 data bytes to DS18B20.	3
Copy Scratchpad	Copies T_H, T_L, and configuration register data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H, T_L, and configuration register data from EEPROM to the scratchpad.	B8h	DS18B20 transmits recall status to master.	
Read Power Supply	Signals DS18B20 power supply mode to the master.	B4h	DS18B20 transmits supply status to master.	

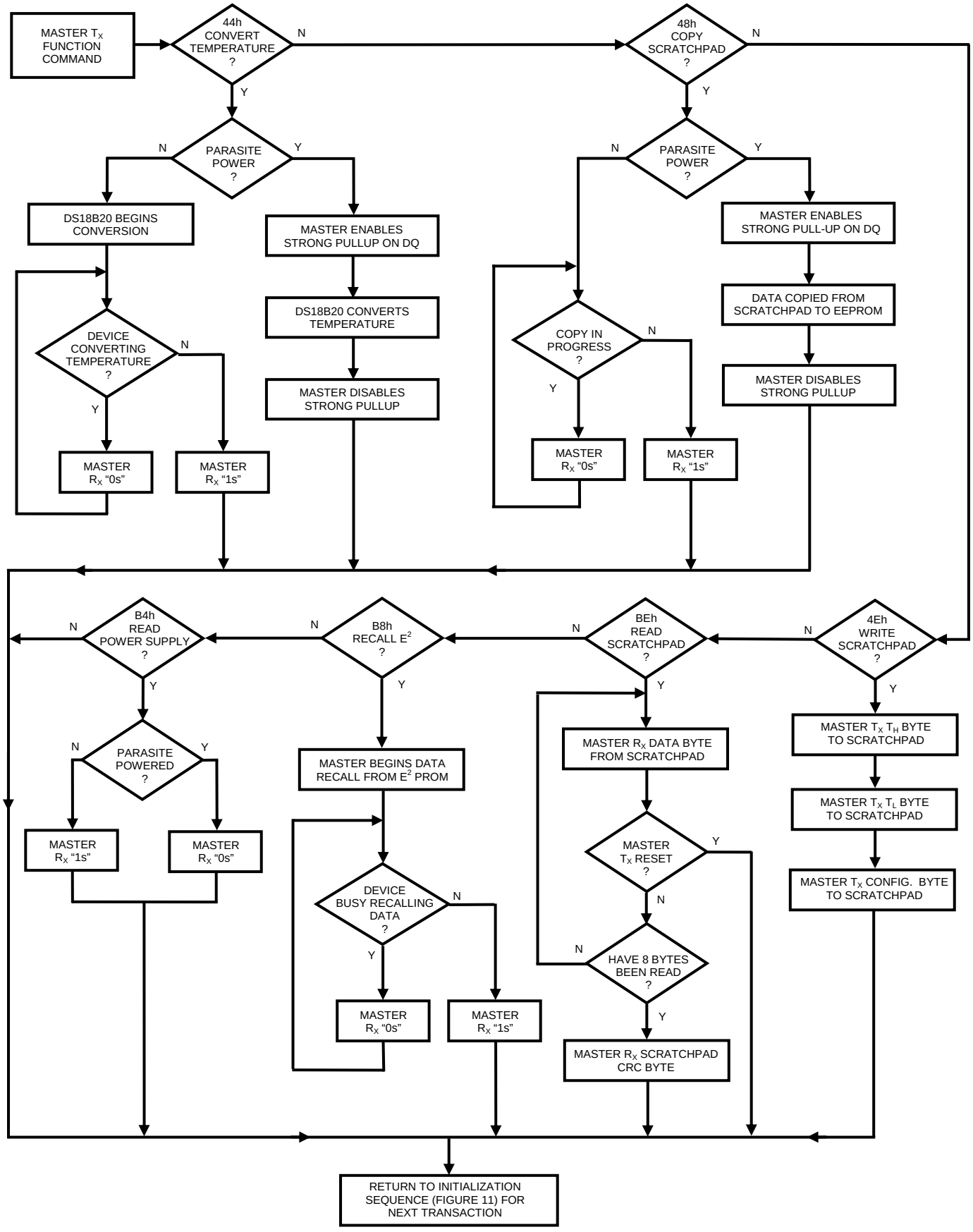
NOTES:

1) For parasite-powered DS18B20s, the master must enable a strong pullup on the 1-Wire bus during temperature conversions and copies from the scratchpad to EEPROM. No other bus activity may take place during this time.
2) The master can interrupt the transmission of data at any time by issuing a reset.
3) All three bytes must be written before a reset is issued.

ROM COMMANDS FLOW CHART Figure 11



DS18B20 FUNCTION COMMANDS FLOW CHART Figure 12



1-WIRE SIGNALING

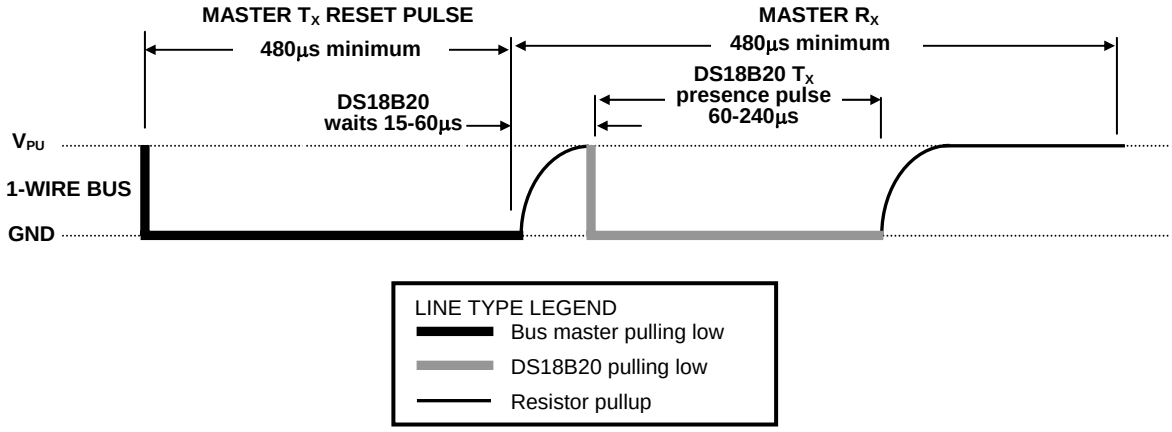
The DS18B20 uses a strict 1-Wire communication protocol to insure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all of these signals, with the exception of the presence pulse.

INITIALIZATION PROCEDURE: RESET AND PRESENCE PULSES

All communication with the DS18B20 begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the DS18B20. This is illustrated in Figure 13. When the DS18B20 sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (T_X) the reset pulse by pulling the 1-Wire bus low for a minimum of 480µs. The bus master then releases the bus and goes into receive mode (R_X). When the bus is released, the 5k pullup resistor pulls the 1-Wire bus high. When the DS18B20 detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.

INITIALIZATION TIMING Figure 13



READ/WRITE TIME SLOTS

The bus master writes data to the DS18B20 during write time slots and reads data from the DS18B20 during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

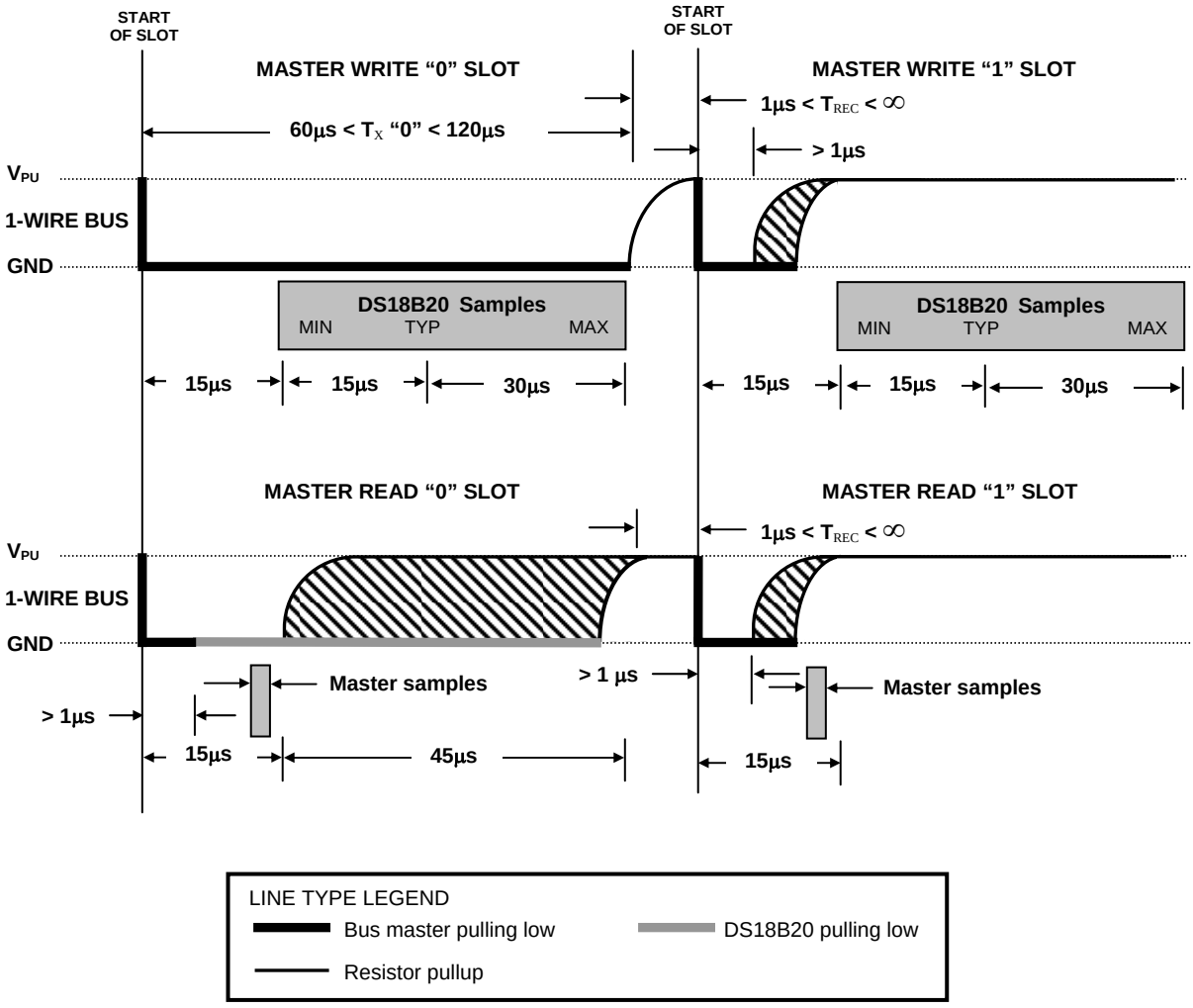
WRITE TIME SLOTS

There are two types of write time slots: “Write 1” time slots and “Write 0” time slots. The bus master uses a Write 1 time slot to write a logic 1 to the DS18B20 and a Write 0 time slot to write a logic 0 to the DS18B20. All write time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (see Figure 14).

To generate a Write 1 time slot, after pulling the 1-Wire bus low, the bus master must release the 1-Wire bus within 15µs. When the bus is released, the 5k pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60µs).

The DS18B20 samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the DS18B20. If the line is low, a 0 is written to the DS18B20.

READ/WRITE TIME SLOT TIMING DIAGRAM Figure 14



READ TIME SLOTS

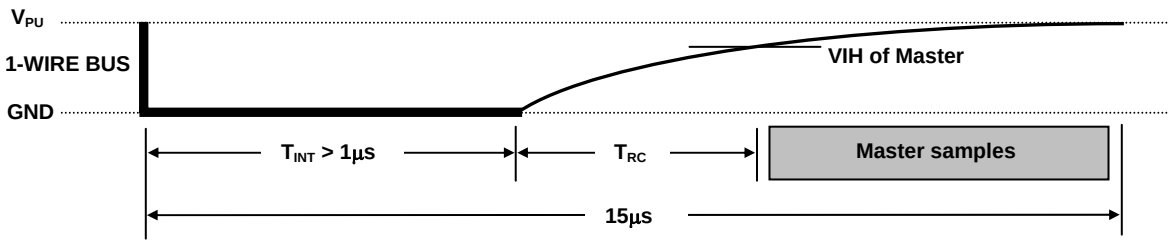
The DS18B20 can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that the DS18B20 can provide the requested data. In addition, the master can generate read time slots after issuing Convert T [44h] or Recall E^2 [B8h] commands to find out the status of the operation as explained in the *DS18B20 FUNCTION COMMAND* section.

All read time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing the bus (see Figure 14). After the master initiates the read time slot, the DS18B20 will begin transmitting a 1 or 0 on bus. The DS18B20 transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the DS18B20 will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resister. Output

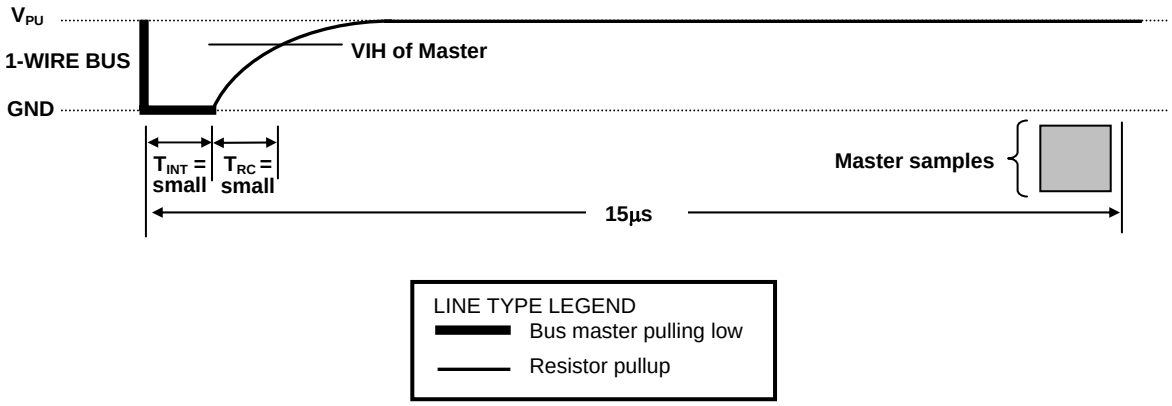
data from the DS18B20 is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot.

Figure 15 illustrates that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs for a read time slot. Figure 16 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as short as possible and by locating the master sample time during read time slots towards the end of the 15µs period.

DETAILED MASTER READ 1 TIMING Figure 15



RECOMMENDED MASTER READ 1 TIMING Figure 16



RELATED APPLICATION NOTES

The following Application Notes can be applied to the DS18B20. These notes can be obtained from the Maxim website at http://www.maxim-ic.com, or through our faxback service at (214) 450–0441.

Application Note 27: Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Product
Application Note 122: Using Dallas' 1-Wire ICs in 1-Cell Li-Ion Battery Packs with Low-Side N-Channel Safety FETs Master
Application Note 126: 1-Wire Communication Through Software
Application Note 162: Interfacing the DS18X20/DS1822 1-Wire Temperature Sensor in a Microcontroller Environment
App Note 208: Curve Fitting the Error of a Bandgap-Based Digital Temperature Sensor
App Note 2420: 1-Wire Communication with a Microchip PICmicro Microcontroller
App Note 3754: Single-Wire Serial Bus Carries Isolated Power and Data

Sample 1-Wire subroutines that can be used in conjunction with AN74 can be downloaded from the Maxim website.

DS18B20 OPERATION EXAMPLE 1

In this example there are multiple DS18B20s on the bus and they are using parasite power. The bus master initiates a temperature conversion in a specific DS18B20 and then reads its scratchpad and recalculates the CRC to verify the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20s respond with presence pulse.
TX	55h	Master issues Match ROM command.
TX	64-bit ROM code	Master sends DS18B20 ROM code.
TX	44h	Master issues Convert T command.
TX	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{conv}).
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20s respond with presence pulse.
TX	55h	Master issues Match ROM command.
TX	64-bit ROM code	Master sends DS18B20 ROM code.
TX	BEh	Master issues Read Scratchpad command.
RX	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.

DS18B20 OPERATION EXAMPLE 2

In this example there is only one DS18B20 on the bus and it is using parasite power. The master writes to the T_H, T_L, and configuration registers in the DS18B20 scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20 responds with presence pulse.
TX	CCh	Master issues Skip ROM command.
TX	4Eh	Master issues Write Scratchpad command.
TX	3 data bytes	Master sends three data bytes to scratchpad (T_H, T_L, and config).
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20 responds with presence pulse.
TX	CCh	Master issues Skip ROM command.
TX	BEh	Master issues Read Scratchpad command.
RX	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.
TX	Reset	Master issues reset pulse.
RX	Presence	DS18B20 responds with presence pulse.
TX	CCh	Master issues Skip ROM command.
TX	48h	Master issues Copy Scratchpad command.
TX	DQ line held high by strong pullup	Master applies strong pullup to DQ for at least 10ms while copy operation is in progress.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.5V to +6.0V
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-55°C to +125°C
Solder Temperature	See IPC/JEDEC J-STD-020A

**These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

DC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; V_{DD}=3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	Local Power	+3.0		+5.5	V	1
Pullup Supply Voltage	V_{PU}	Parasite Power	+3.0		+5.5	V	1,2
		Local Power	+3.0		V_{DD}		
Thermometer Error	t_{ERR}	-10°C to +85°C			±0.5	°C	3
		-55°C to +125°C			±2		
Input Logic Low	V_{IL}		-0.3		+0.8	V	1,4,5
Input Logic High	V_{IH}	Local Power	+2.2		The lower of 5.5 or V_{DD} + 0.3	V	1, 6
		Parasite Power	+3.0				
Sink Current	I_L	$V_{I/O}$=0.4V	4.0			mA	1
Standby Current	I_{DDS}			750	1000	nA	7,8
Active Current	I_{DD}	V_{DD}=5V		1	1.5	mA	9
DQ Input Current	I_{DQ}			5		µA	10
Drift				±0.2		°C	11

NOTES:

1) All voltages are referenced to ground.
2) The Pullup Supply Voltage specification assumes that the pullup device is ideal, and therefore the high level of the pullup is equal to V_{PU}. In order to meet the V_{IH} spec of the DS18B20, the actual supply rail for the strong pullup transistor must include margin for the voltage drop across the transistor when it is turned on; thus: $V_{PU\_ACTUAL} = V_{PU\_IDEAL} + V_{TRANSISTOR}$.
3) See typical performance curve in Figure 17
4) Logic low voltages are specified at a sink current of 4mA.
5) To guarantee a presence pulse under low voltage parasite power conditions, V_{ILMAX} may have to be reduced to as low as 0.5V.
6) Logic high voltages are specified at a source current of 1mA.
7) Standby current specified up to 70°C. Standby current typically is 3µA at 125°C.
8) To minimize I_{DDS}, DQ should be within the following ranges: GND ≤ DQ ≤ GND + 0.3V or V_{DD} – 0.3V ≤ DQ ≤ V_{DD}.
9) Active current refers to supply current during active temperature conversions or EEPROM writes.
10) DQ line is high (“hi-Z” state).
11) Drift data is based on a 1000 hour stress test at 125°C with V_{DD} = 5.5V.

AC ELECTRICAL CHARACTERISTICS: NV MEMORY

(-55°C to +100°C; V_{DD} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
NV Write Cycle Time	t_{wr}			2	10	ms
EEPROM Writes	N_{EEWR}	-55°C to +55°C	50k			writes
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years

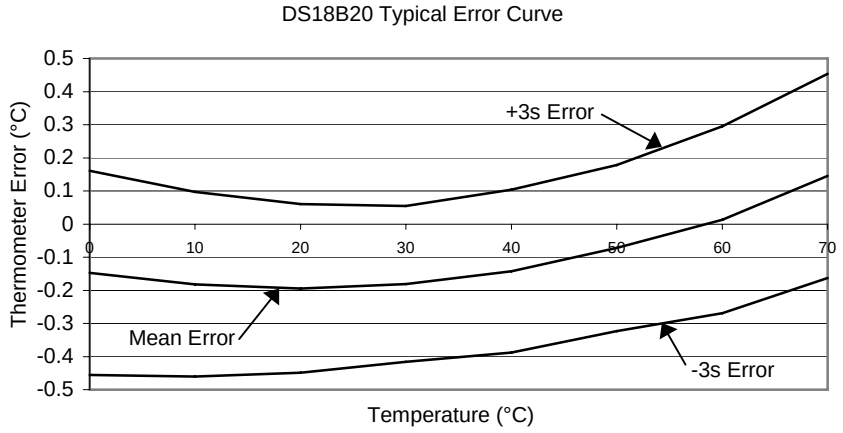
AC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; V_{DD} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}	9-bit resolution			93.75	ms	1
		10-bit resolution			187.5	ms	1
		11-bit resolution			375	ms	1
		12-bit resolution			750	ms	1
Time to Strong Pullup On	t_{SPON}	Start Convert T Command Issued			10	µs	
Time Slot	t_{SLOT}		60		120	µs	1
Recovery Time	t_{REC}		1			µs	1
Write 0 Low Time	r_{LOW0}		60		120	µs	1
Write 1 Low Time	t_{LOW1}		1		15	µs	1
Read Data Valid	t_{RDV}				15	µs	1
Reset Time High	t_{RSTH}		480			µs	1
Reset Time Low	t_{RSTL}		480			µs	1,2
Presence Detect High	t_{PDHIGH}		15		60	µs	1
Presence Detect Low	t_{PDLOW}		60		240	µs	1
Capacitance	$C_{IN/OUT}$				25	pF	

NOTES:

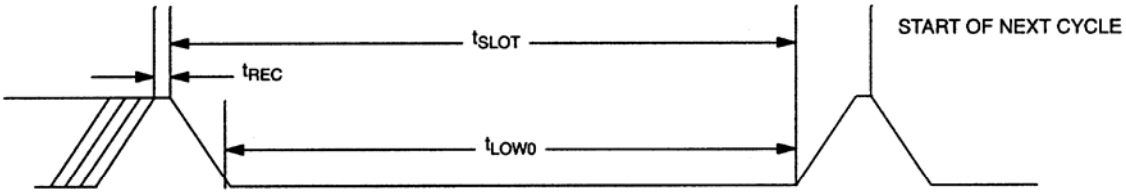
1) Refer to timing diagrams in Figure 18.
2) Under parasite power, if t_{RSTL} > 960µs, a power on reset may occur.

TYPICAL PERFORMANCE CURVE Figure 17

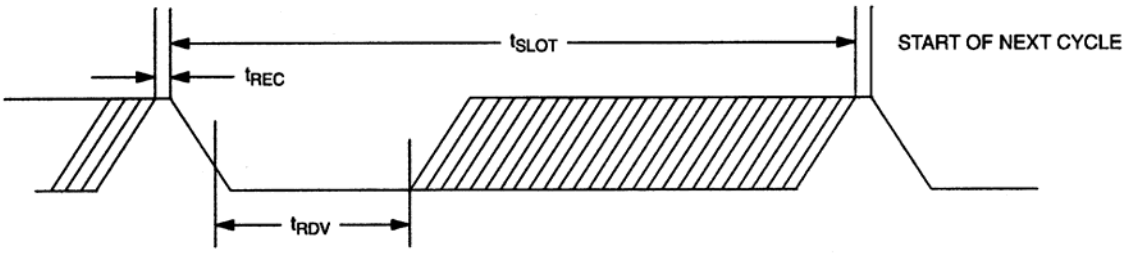


TIMING DIAGRAMS Figure 18

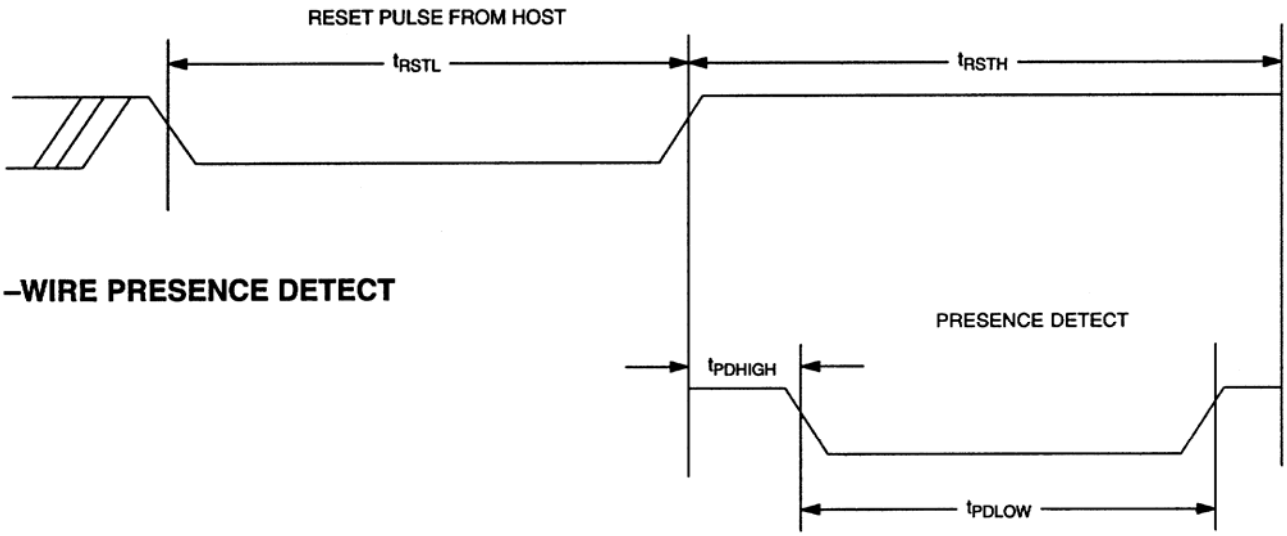
1–WIRE WRITE ZERO TIME SLOT



1–WIRE READ ZERO TIME SLOT



1–WIRE RESET PULSE



1–WIRE PRESENCE DETECT