RANCANG BANGUN PENGAMAN PINTU RUMAH OTOMATIS MENGGUNAKAN E-KTP BERBASIS MIKROKONTROLLER

SKRIPSI

Diajukan Sebagai Salah Satu Syarat untuk Mencapai Gelar

SARJANA

Pada Program Studi Sistem Komputer

IIB Darmajaya Bandar Lampung

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PERNYATAAN ORISINILITAS PENELITIAN

PERNYATAAN

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"Selama nyawa masih di raga, semangat masih membara, tubuh masih kuat untuk bergerak, teruslah berjuang"

(Orang Tua Tercinta)

"Tetaplah Hidup, Walau tidak berguna"

(Adam Feiga Hadinata)

ABSTRAK

RANCANG BANGUN PENGAMAN PINTU RUMAH OTOMATIS MENGGUNAKAN E-KTP BERBASIS MIKROKONTROLLER

Oleh

Adam Feiga Hadinata

Sistem pengunci pintu saat ini masih menggunakan kunci konvensional, sehingga dirasa kurang efisien untuk rumah yang isinya banyak sekali barang-barang berharga dengan pintu yang menjadi akses utama untuk masuk kedalam rumah, selain itu kunci konvensional mudah dibuka oleh pencuri. Sehingga diperlukan kunci yang lebih praktis dan efisien namun tetap aman, dari masalah tersebut penulis mempunyai gagasan untuk menghasilkan alat pengaman pintu yang aman dan praktis berbasis RFID dengan memanfaatkan E-KTP sebagai kunci pada pengaman pintu rumah. Oleh karena itu peneiti ingin membuat Rancang Bangun Pengaman Pintu Rumah Otomatis Menggunakan E-KTP Berbasis Mikrokontroller sebagai pengendali rangkaian. Penelitian ini menggunakan metode *Research and Development* yaitu metode yang bertujuan menghasilkan atau mengembangkan produk tertentu. Metode ini diterapkan pada prosedur penelitian menjadi 5 tahap yaitu (1) Studi Literatur, (2) Analisis Kebutuhan Sistem, (3) Perakitan, (4) Pengujian Sistem, (5) Analisa Kerja. Berdasarkan hasil pengujian dapat disimpulkan bahwa simulasi alat pengaman pintu dapat beroperasi dengan baik, sesuai rancangan yang dibuat. RFID *reader* yang digunakan memiliki frekuensi 13,56 MHz diletakkan diluar Rumah dapat membaca ID e-KTP dengan jarak maksimal 2cm. *Selenoid Door Lock* dapat membuka kunci pintu apabila ID e-KTP sesuai dengan data yang tersimpan pada Arduino Uno, *Selenoid Door Lock* akan mengunci kembali dalam waktu 5 detik. Apabila pemilik rumah hendak masuk namun kehilangan E-KTP nya, pemilik rumah masih bisa membuka *Door Lock* dengan perintah SMS yang dikirimkan ke GSM Shield, dari dalam rumah ditambahkan Sensor Touch sebagai pembuka Door Lock karena E-KTP hanya berfungsi sebagai pembuka Door Lock dari luar rumah

Kata Kunci : E-KTP, Mikrokontroler Arduino Uno, RFID *reader, Selenoid Doorlock,* Sensor *Touch*

ABSTRACT

DESIGN OF E-ID-BASED AUTOMATIC HOUSE DOOR USING MICROCONTROLLER-

By:

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The current door locking system still uses conventional keys, so it is considered inefficient for a house that contains a lot of valuables with a door that is the main access to enter the house, besides that a conventional key is easily opened by thieves. Therefore, we need a key that is more practical and efficient but still safe, from this problem the authors have the idea to produce a safe and practical door-based RFID security tool by using E-ID as a key on the door security of the house. Therefore, the researcher wanted to create an Automatic Home Door Safety Building Design Using Microcontroller based E-ID as the circuit controller. This research used the research and development method which is a method that aims to produce or develop certain products. This method was applied to the research procedure into 5 stages, namely (1) Literature Study, (2) Systems Requirement Analysis, (3) Assembling, (4) System Testing, (5) Work Analysis. Based on the test results it can be concluded that the simulation of the safety door can operate properly, according to the design made. RFID reader that is used has a frequency of 13.56 MHz placed outside the House can read e-KTP IDs with a maximum distance of 2cm.

Selenoid Door Lock can open a door lock if the e-KTP ID matches the data stored on Arduino Uno, Selenoid Door Lock will lock again within 5 seconds. If the homeowner wants to enter but loses his E-KTP, the homeowner can still open the Door Lock with an SMS command sent to the GSM Shield, adding a Touch Sensor from the house to open the Door Lock because the E-KTP only functions as a Door Lock opener from outside home

Keywords: E-ID, Arduino Uno Microcontroller, RFID reader, Doorlock Selenoid, Touch Sensor

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Adam Feiga Hadinata

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Daftar Isi

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BAB I
PENDAHULUAN

1.1 Latar Belakang

Kunci pintu merupakan keamanan mutlak yang berada pada setiap rumah khususnya pada bagian pintu, namun kunci pintu yang ada sekarang ini masih kurang efisien dalam penggunaannya dikarenakan setiap hendak membuka maupun mengunci, pemilik masih sibuk mencari kunci untuk mengunci ataupun membuka pintu, kunci konvensional ini dirasa kurang efisien. Oleh karena itu peneliti tergerak untuk membuat kunci elektronik menggunakan *E-KTP* agar lebih efisien dalam penggunaannya.

Sistem pengamanan yang digunakan saat ini masih menggunakan analog, sehingga perlu diganti menggunakan sistem digital untuk meningkatkan sistem keamanan namun efisien dalam penggunaannya. Penggunaan sistem kendali elektronik hampir mencangkup sebagian besar kehidupan sehari-hari manusia sekarang ini. Sistem kendali elektronik bersifat praktis dan efisien, sehingga banyak orang yang mulai menggunakannya. Sistem kendali elektronik ada untuk menggantikan atau menambah sistem yang ada karena sistem keamanan digital memiliki kelebihan, yaitu praktis, efisien, mudah di aplikasikan, serta lebih *futuristic.*

Dalam membuat sistem keamanan berupa kunci elektronik peneliti menggunakan beberapa komponen yaitu: menggunakan RFID yang digunakan sebagain inputan untuk dapat membaca card E-KTP yang akan digunakan untuk membuka kunci kemudian peneliti menggunakan Arduino Uno yang digunakan sebagai pemeroses dari keseluruhan sistem sehingga jika terjadi E-KTP asing mencoba untuk mengakses sistem dapat memberikan informasi melalui pesan SMS (*Short Massage Service)*, peneliti juga menambahkan alternatif apabila pemilik rumah hendak masuk rumah namun kehilangan E-KTP nya, pemilik rumah masih tetap

bisa masuk dengan adanya perintah melalui SMS untuk membuka kunci elektronik yang ada pada pintu.

Dari permasalahan diatas, maka peneliti ingin membuat sebuah "Rancang Bangun Pengaman Pintu Rumah Otomatis Menggunakan E-KTP Berbasis Mikrokontroller ". Dalam merancang sistem keamanan pintu rumah menggunakan E-KTP peneliti menggunakan raider RFID sebagai inputan dalam membaca nomor ID pada E-KTP yang akan diproses oleh Arduino Uno sehingga akan menghasilkan outputan menyalakan *Selenoid Doorlock*. Jika E-KTP yang ditempelkan salah sebanyak 1 kali maka *GSM Shield* akan mengirimkan SMS (*Short Massage Service)* kepada pemilik rumah.

1.2 Rumusan Masalah

Berdasarkan dari latar belakang yang telah dikemukakan, maka rumusan masalah dalam penelitian ini, yaitu:

Bagaimana merancang serta membuat sistem yang dapat membuka pintu rumah menggunakan E-KTP serta dapat mengirimkan perintah SMS (*Short Massage Service)* dengan menggunakan arduino uno ?

Bagaimana membuat alternatif apabila pemilik rumah kehilangan E-KTP nya namun hendak masuk kerumah ?

1.3 Ruang Lingkup Penelitian

Berdasarkan dari hasil penelitian yang telah dilakukan, maka ruang lingkup dalam penelitian ini, yaitu;

1. Mikrokontroler yang digunakan adalah *Arduino Uno*
2. Alat ini hanya mambuka kunci yang ada pada pintu.
3. *GSM shield* SIM900A sebagai outputan dalam bentuk pengiriman pesan SMS (*Short Massage Service)* jika E-KTP yang di tempel salah dan sebagai notifikasi apabila pintu telah berhasil di kontrol dengan cara mengirimkan SMS.
4. RFID digunakan sebagai inputan dalam membaca E-KTP.

1.4 Tujuan Penelitian

Tujuan dari pembuatan alat ini yaitu dapat membuat kunci elektronik pintu rumah yang menggunakan 3 *E-KTP* dan SMS dengan sistem relay serta dapat mengirimkan (SMS *Short Massage Service)* jika E-KTP yang ditempelkan salah sebanyak 1 kali.

1.5 Manfaat Penelitian

Manfaat dari penelitian ini adalah

1. Membuat kunci elektronik yang mudah digunakan.
2. Lebih efisien dalam membuka kunci pintu karena pengguna tinggal menempelkan E-KTP pada RFID.
3. Mempermudah ketika hendak membuka kunci pintu dari dalam karena terdapat sensor sentuh.

1.6 Sistematika Penulisan

Sistematika penulisan yang digunakan dalam tugas akhir ini terbagi dalam beberapa pokok bahasan, yaitu :

BAB I PENDAHULUAN

Dalam bab ini berisikan latar belakang masalah, rumusan masalah, batasan masalah, tujuan penelitian dan manfaat penelitian.

BAB II TINJAUAN PUSTAKA

Bab ini berisikan tentang teori – teori yang berkaitan dengan Sistem Pengaman Kendaraan Roda Empat Menggunakan E-KTP Berbasis Mikrokontroler".

BAB III METODOLOGI PENELITIAN

Bab ini menjelaskan apa yang akan digunakan dalam uji coba pembuatan alat, tahapan peracangan dari alat, diagaram blok dari alat, dan cara kerja alat tersebut.

BAB IV HASIL DAN PEMBAHASAN

Bab ini berisi tentang implementasi alur, analisis dan pembahasan dari alur yang dirancang.

BAB V SIMPULAN DAN SARAN

Bab ini berisikan kesimpulan dari pengujian sistem serta saran apakah rangkaian ini dapat digunakan secara tepat dan dikembangkan perakitannya.

DAFTAR PUSTAKA

LAMPIRAN

BAB II
TINJAUAN PUSTAKA

2.1 Studi Literatur

Penelitian tentang menyalakan kunci pintu elektronik menggunakan E-KTP sudah pernah dilakukan oleh beberapa peneliti. Ringakasan Studi Literatur yang dilakukan untuk mengetahui sejauh mana penelitian yang sudah ada dapat dilihat sebagai berikut:

1. (Saputro, 2016) dengan judul Rancang Bangun Pengaman Pintu Otomatis Menggunakan E-KTP Berbasis Mikrokontroler Atmega328 sistem kerja dari alat ini yaitu RFID reader yang digunakan memiliki frekuensi 13,56 MHz yang diletakkan dalam box dengan tebal 2mm dapat membaca ID E-KTP dengan jarak maksimal 1,8 cm. Solenoid dapat membuka pengunci pintu apabila ID E-KTP sesuai dengan memori mikrokontroler ATmega328, solenoid akan mengunci kembali dalam waktu 10 detik Alat pengaman pintu otomatis menggunakan E-KTP ini mampu membaca ID E-KTP dengan jarak maksimal 1.8cm dengan sensor RFID *reader* MFRC522 yang memiliki frekuensi 13,56 MHz.

2. (Hermawan, 2016) dengan judul perancangan dan pembuatan kunci pintu rumah menggunakan RFID dengan multi reader berbasis Arduino sistem kerja alat ini ialah dua buah reader RFID digunakan untuk membaca data pada Tag. Penggunaan dua buah reader dimaksudkan agar selain ID tag, kunci juga di kendalikan dengan suatu kode unik yang berupa pola pembacaan tag dengan dua reader tersebut. Alat ini juga dilengkapi dengan Lcd 16x2 dan LED RGB yang digunakan sebagai penampil indikator proses. Mikro servo merupakan bagian mekanik dari alat ini, mikro servo akan aktif apabila mendapat perintah dari sistem. Pengguna dapat menggunakan alat pengunci pintu ini dengan cara mendekatkan Tag RFID pada masing-masing reader, dengan pola pembacaan tertentu. Jika UID dan kode sama dengan database maka sistem akan mengaktifkan servo.

3. (Astono, 2006) dengan judul implementasi dan perancangan kunci pintu hotel dengan *Radio Frecuency Identification (RFID)* cara kerja kunci pintu dengan RFID adalah tag RFID dibaca oleg reader, kemudian data serial (ID) dikirim reader ke mikrokontroler. Dalam mikrokontroler data yang diterima digabungkan, kemudian dibandingkan dengan data yang tersimpan dalam memori mikrokontroler. Jika ID tag RFID sesuai dengan ID yang tersimpan dalam memori maka mikrokontroler akan mengaktifkan relay solenoid. LCD digunakan untuk memonitoring kerja sistem. Solenoid digunakan sebagai pengganti kunci pintu manual. Sedangkan keypad digunakan untuk mengganti tag RFID (kunci) dengan memasukkan ID tag yang baru yang tertulis di badan tag RFID. RFID reader (ID-10) mampu membaca pada jarak maksimum 6 cm.

4. (Hendra, 2017) dengan judul perancangan teknologi prototype RFID dan keypad 4x4 untuk keamanan ganda pada rumah dengan Hasil pengujian menunjukkan RFID Reader mampu bekerja dengan baik. RFID dapat membaca data dari kartu RFID dengan jarak maksimal 7cm dan menampilkannya pada LCD, Keypad sebagai alat input password untuk membuka pengunci loker dapat berfungsi dengan baik, Motor servo sebagai tuas pintu sebagai penggerak untuk menutup dan membuka pintu rumah dapat bekerja secara otomatis.

5. (Irawan, 2016) dengan judul pengembangan kunci elektronik menggunakan RFID dengan sistem IOT Prinsip kerja dari sistem pemanfaatan IoT dalam proses monitoring tersebut adalah diawali dengan proses pembacaan kunci elektronik yang berupa kartu RFID yang dibawa penghuni rumah, pada saat pembacaan kartu kamera akan merekam gambar dan data kartu dicocokkan dengan database, jika data cocok maka pintu akan terbuka, akan tetapi jika tidak cocok akan muncul peringatan kepada pemilik melalui jaringan internet, dengan menggunakan sistem ini proses monitoring menjadi lebih mudah karena dapat dilakukan kapan saja dan dari mana saja karena memanfaatkan jaringan internet. dengan hasil pengujian

didapatkan jarak maksimal dari pembacaan RFID adalah 6 cm, tetapi yang yang terbaik adalah 5 cm, seperti dapat dilihat pada tabel 1. Hal ini disebabkan pada reader tidak dipasang external antena, jika dipasang external antena maka akan didapat jarak maksimal sampai 25 cm.

2.2 Dasar Teori

2.2.1 Sistem

Sistem berasal dari bahasa Latin (*systema*) dan bahasa Yunani (*sustema*) adalah suatu kesatuan yang terdiri dari komponen atau elemen yang dihubungkan bersama untuk memudahkan aliran informasi, materi atau energy untuk mencapai suatu tujuan. Istilah ini sering dipergunakan untuk menggambarkan suatu setentitas yang berinteraksi, dimana suatu model matematika seringkali biasa dibuat. Sistem juga merupakan kesatuan bagian-bagian yang saling berhubungan yang berada dalam suatu wilayah serta memiliki item-item penggerak, contoh umum misalnya seperti negara. Negara merupakan kumpulan dari beberapa elemen kesatuan lain seperti provinsi yang saling berhubungan sehingga membentuk suatu negara yang berperan sebagai penggeraknya yaitu rakyat yang berada dinegara tersebut. Kata "sistem" banyak sekali digunakan dalam percakapan sehari-hari, dalam forum diskusi maupun dokumen ilmiah. Kata ini digunakan untuk banyak hal, dan pada banyak bidang pula, sehingga maknanya menjadi beragam. Dalam pengertian yang paling umum, sebuah sistem adalah sekumpulan benda yang memiliki hubungan di antara mereka (Sidarta, 2016).

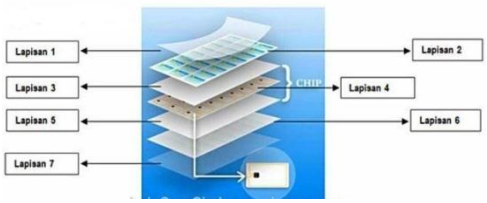
2.2.2 Pengertian Keamanan

Keamanan adalah keadaan bebas dari bahaya. Istilah ini bisa digunakan dengan hubungan kepada kejadian yang tidak diinginkan, dan lain-lain. Keamanan merupakan topik yang luas termasuk keamanan nasional terhadap serangan teroris, keamanan komputer terhadap *hacker* atau *cracker*, keamanan rumah terhadap maling dan penyelusup lainnya. Kebutuhan dasar manusia prioritas kedua berdasarkan kebutuhan fisiologis dalam hirarki *Maslow* yang harus terpenuhi selama hidupnya, sebab dengan terpenuhinya rasa aman setiap individu dapat berkarya dengan optimal dalam hidupnya. Mencari lingkungan yang betul-

betul aman memang sulit, maka konsekuensinya promosi keamanan berupa kesadaran dan penjagaan adalah hal yang penting. Keamanan fisik *(Biologic safety)* merupakan keadaan fisik yang aman terbebas dari ancaman kecelakaan dan cedera *(injury)* baik secara mekanis, thermis, elektris 12 maupun bakteriologis. Kebutuhan keamanan fisik merupakan kebutuhan untuk melindungi diri dari bahaya yang mengancam kesehatan fisik, yang pada pembahasan ini akan difokuskan pada providing for safety atau memberikan lingkungan yang aman . (Sutris, 2015).

2.2.3 Kelebihan E-KTP Sebagai Tag Pasif

Bahan fisik *chip* yang tipis seperti kertas didominasi oleh silikon dan jenis plastik, tidak tahan panas, korosi, basah atau lembab. *Chip* E-KTP menggunakan antar muka nirsentuh (*contactless*) yang memenuhi standar ISO 14443 A/B. Transmisi data melalui gelombang radio. Blangko *e*-KTP terbuat dari bahan PETG, semacam polimer termoplastik, yang tersusun dalam 7 lapisan.



Gambar 2.1 Lapisan e-KTP

E-KTP sendiri secara mekanisme teknis memiliki keuntungan:

1. *Chip e*-KTP dilindungi, salah satunya, dengan mekanisme autentikasi dua arah, yaitu suatu mekanisme untuk saling mengenali antara *chip e*-KTP dengan *reader* RFID, di mana *chip* harus dapat mengenali *reader* RFID (arah 1) dan *reader* RFID harus dapat mengenali *chip* (arah 2), setelah melalui mekanisme autentikasi ini maka data yang tersimpan di dalam chip baru dapat dibaca oleh *reader* RFID.
2. *Reader* RFID menghasilkan medan radio frekuensi tinggi untuk memberikan pasokan daya yang sesuai dengan kebutuhan *chip e*-KTP, di mana medan medan radio tersebut akan dimodulasikan untuk keperluan komunikasi.

3. Kisaran dari besar medan magnet frekuensi radio yang dihasilkan oleh *reader* RFID adalah mengikuti ketentuan dalam ISO/IEC 14443, yaitu antara 1,5 A/m sampai dengan 7,5 A/m. Sedangkan besar frekuensi dari modulasi amplitudo medan magnet tersebut, yang digunakan untuk mengirimkan data ke *chip e*-KTP, adalah 13,56 MHz.

4. *Chip* yang tertanam dalam kartu ini memungkinnya melakukan berbagai proses komputasi yang tidak dapat dilakukan oleh kartu berbasis *magnetic stripe*. Dengan kemampuan ini, kartu *chip* dapat menjalankan berbagai algoritma dan protokol keamanan yang cukup kompleks.

2.3 Perangkat Keras Yang Digunakan

2.3.1 *Radio Frequency Identification (RFID)*

Radio Frequency Identification (RFID) adalah teknologi identifikasi yang mudah digunakan,. *RFID* mengkombinasikan keunggulan yang tidak tersedia pada teknologi identifikasi yang lain. *RFID* disediakan dalam device yang hanya dapat dibaca saja (*Read Only*) atau dapat dibaca dan ditulis (*Read/Write*), tidak memerlukan kontak langsung untuk dapat beroperasi, dapat berfungsi pada berbagai variasi kondisi lingkungan, dan menyediakan tingkat integritas yang tinggi. Sebagai tambahan, karena teknologi ini sulit untuk dipalsukan, maka *RFID* dapat menyediakan tingkat keamanan yang tinggi.

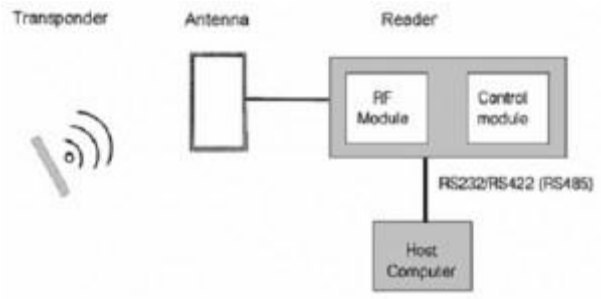
Pada sistem *RFID* umumnya, tag atau transponder ditempelkan pada suatu objek. Setiap tag dapat membawa informasi yang unik, di antaranya: serial number, model, warna, dan data lain dari objek tersebut. Ketika tag ini melalui medan yang dihasilkan oleh pembaca *RFID* yang kompatibel, tag akan mentransmisikan informasi yang ada pada tag kepada pembaca *RFID*, sehingga proses identifikasi objek dapat dilakukan.

Sistem *RFID* terdiri dari empat komponen, di antaranya sebagai berikut :

1. Tag: Ini adalah *device* yang menyimpan informasi untuk identifikasi objek. Tag *RFID* sering juga disebut sebagai transponder.

2. Antena: untuk mentransmisikan sinyal frekuensi radio antara pembaca *RFID* dengan tag *RFID.* Pembaca *RFID:* adalah device yang kompatibel dengan tag *RFID* yang akan berkomunikasi secara wireless dengan tag.
3. Software Aplikasi: adalah aplikasi pada sebuah workstation atau PC yang dapat membaca data dari tag melalui pembaca *RFID.* Baik tag dan pembaca *RFID* diperlengkapi dengan antena sehingga dapat menerima dan memancarkan gelombang elektromagnetik.

2.3.2 Sistem *RFID*



Gambar 2.2. Sistem *RFID*

(Sumber https://www.elektronikar,2014)

2.3.2.1 Pembaca *RFID*

Sebuah pembaca *RFID* harus menyelesaikan dua buah tugas, yaitu:

1. Menerima perintah dari *software* aplikasi
2. Berkomunikasi dengan tag *RFID*

Pembaca *RFID* adalah merupakan penghubung antara *software* aplikasi dengan antena yang akan meradiasikan gelombang radio ke tag *RFID*. Gelombang radio yang diemisikan oleh antena berpropagasi pada ruangan di sekitarnya. Akibatnya data dapat berpindah secara wireless ke tag *RFID* yang berada berdekatan dengan antena.

2.3.2.2 Tag *RFID*

Tag *RFID* adalah *device* yang dibuat dari rangkaian elektronika dan antena yang terintegrasi di dalam rangkaian tersebut. Rangkaian elektronik dari tag *RFID*

umumnya memiliki memori sehingga tag ini mempunyai kemampuan untuk menyimpan data. Memori pada tag secara dibagi menjadi sel-sel. Beberapa sel menyimpan data *Read Only*, misalnya serial number yang unik yang disimpan pada saat tag tersebut diproduksi. Sel lain pada *RFID* mungkin juga dapat ditulis dan dibaca secara berulang.

Berdasarkan catu daya tag, tag *RFID* dapat digolongkan menjadi:

1. Tag Aktif: yaitu tag yang catu dayanya diperoleh dari batere, sehingga akan mengurangi daya yang diperlukan oleh pembaca *RFID* dan tag dapat mengirimkan informasi dalam jarak yang lebih jauh. Kelemahan dari tipe tag ini adalah harganya yang mahal dan ukurannya yang lebih besar karena lebih komplek. Semakin banyak fungsi yang dapat dilakukan oleh tag *RFID* maka rangkaiannya akan semakin komplek dan ukurannya akan semakin besar.
2. Tag Pasif: yaitu tag yang catu dayanya diperoleh dari medan yang dihasilkan oleh pembaca *RFID*. Rangkaiannya lebih sederhana, harganya jauh lebih murah, ukurannya kecil, dan lebih ringan. Kelemahannya adalah tag hanya dapat mengirimkan informasi dalam jarak yang dekat dan pembaca *RFID* harus menyediakan daya tambahan untuk tag *RFID*.

Tag *RFID* telah sering dipertimbangkan untuk digunakan sebagai barcode pada masa yang akan datang. Pembacaan informasi pada tag RFID tidak memerlukan kontak sama sekali. maka tag *RFID* dapat menyimpan jauh lebih banyak informasi dibandingkan dengan *barcode*. Fitur pembacaan jamak pada teknologi RFID sering disebut sebagai *anti collision.*

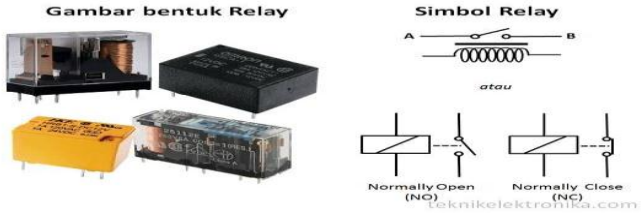
2.3.3 *Relay*

Relay merupakan bentuk hambatan terdiri atas titik-titik kontak bawah dengan gulungan *spool*-nya tidak bergerak dan titik kontak bagian atas yang bergerak. Prinsip kerja hambatan adalah menghubungkan titik-titik kontak bagian bawah dengan titik bagian atas yaitu terletak gulungan *spool* dialiri arus listrik yang timbul elektromagnet. *Relay* merupakan bentuk hambatan terdiri atas titik-titik

kontak bawah dengan gulungan *spool*-nya tidak bergerak dan titik kontak bagian atas yang bergerak. Prinsip kerja hambatan adalah menghubungkan titik-titik kontak bagian bawah dengan titik bagian atas yaitu terletak gulungan *spool* dialiri arus listrik yang timbul elektromagnet.Secara sederhana relay elektromekanis ini didefinisikan sebagai berikut :

1. Alat yang menggunakan gaya elektromagnetik untuk menutup/membuka saklar
2. Saklar yang digerakkan (secara mekanis) oleh daya/energi listrik.

Dibawah ini adalah gambar fisik, bentuk dan Simbol Relay yang sering ditemukan di Rangkaian Elektronika.



Gambar 2.3 Gambar dan Simbol Relay

(http://teknikelektronika.com/pengertian-relay-fungsi-relay/)

Gambar 2.4 Relay

(Sumber : Kilian, Christopher T, Modern Control Technology, (West Published Co : 1996)

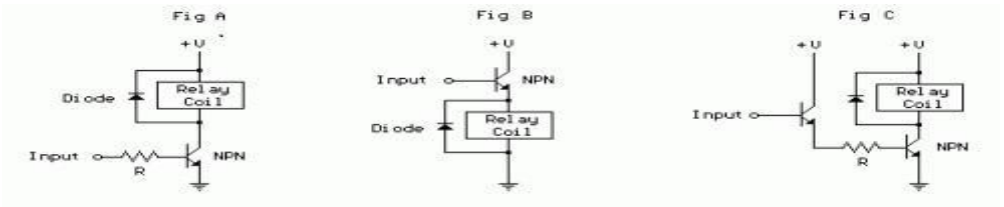
Bagian titik kontak dibagi menjadi 2 bagian yaitu bagian kontak utama dan kontak bantu yaitu : Bagian kontak utama gunanya untuk menghubungkan dan memutuskan arus listrik bagian yang menuju beban/pemakai.Bagian kontak bantu gunanya untuk menghubungkan dan memutuskan arus listrik ke bagian yang menuju bagian pengendali. Kontak Bantu mempunyai 2 kontak yaitu kontak hubung (NC) dan kontak putus (NO) menandakan masing-masing kontak dan gulungan spool.Secara umum, relay digunakan untuk memenuhi fungsi–fungsi berikut :

1. Remote control : dapat menyalakan atau mematikan alat dari jarak jauh.
2. Penguatan daya : menguatkan arus atau tegangan.

3. Pengatur logika kontrol suatu sistem. Susunan kontak pada relay adalah:
4. Normally Open : Relay akan menutup bila dialiri arus listrik.
5. Normally Close : Relay akan membuka bila dialiri arus listrik.
6. Changeover : Relay ini memiliki kontak tengah yang akan melepaskan diri dan membuat kontak lainnya berhubungan..

2.3.3.1 *Interface Driver Relay*

Penggunaan *relay* sering menjadi pilihan karena *relay* mudah dikontrol, *relay* dapat diberi beban yang besar baik beban AC maupun DC, dan sebagai isolator yang baik antara rangkaian beban dengan rangkaian kendali. Rangkaian *interface relay* dpat dibangun menggunakan konsep transistor sebagai saklar. Transistor yang digunakan untuk *driver relay* dapat dikonfigurasikan dengan *common emitor*, *emitor follower* atau transistor *darlington*. Teknik *interface* antara *relay* dengan rangkaian digital atau rangkaian *microcontroller* dapat dilihat pada gambar dibawah ini :



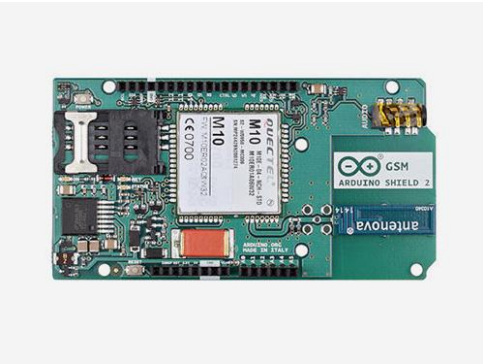
Gambar 2.5 Rangkaian Interface Driver Relay

(http://elektronika-dasar.web.id/teori-elektronika/interface-relay-ke-rangkaian- digital)

Rangkaian *inteface* antar *relay* dengan rangkaian digital pada gambar diatas ada 3 jenis interface yang dapat digunakan. Bagian dan fungsi komponen dari rangkaian *interface relay* diatas sebagai berikut :

1. Rangkaian pada gambar A, rangkaian pada gambar A tersebut menggunakan mode *common emitor*, apabila basis mendapat sinyal *input* logika 1 (sumber tegangan positif) maka transistor pada gambar A akan mendapat bias maju, sehingga transistor ON dan memberikan sumber tegangan ke *relay* dan *relay* menjadi ON.
2. Rangkaian pada gambar B adalah *interface relay* yang menggunakan transistor teknik *emior folower* dimana *relay* diletakan pada kaki emitor trnasistor. Fungsi dioda yang dipasangkan pada rangkaian *interface* tersebut digunakan untuk menyerap tegangan induksi yang dihasilkan oleh *relay*.
3. Rangkaian pada gambar C merupakan teknik *inteface relay* ke rangkaian digital menggunakan transistor yang dirangkai secara *darlington*.

2.3.4 *GSM Shield SIM900*



Gambar 2.6 *GSM Shield (GSM)*

(Sumber https:// www.elektronika.cc.com)

Arduino *GSM Shield* V2 menghubungkan Arduino Anda ke internet menggunakan jaringan nirkabel GPRS. Cukup colokkan modul ini ke papan Arduino Anda, pasang kartu SIM dari operator yang menawarkan jangkauan GPRS dan ikuti beberapa petunjuk sederhana untuk mulai mengendalikan dunia Anda melalui internet. Anda juga dapat membuat / menerima panggilan suara menggunakan jack audio / mikrofon on-board dan mengirim / menerima pesan SMS. Arduino *GSM Shield* 2 memungkinkan dewan Arduino terhubung ke internet, membuat / menerima panggilan suara dan mengirim / menerima pesan SMS. Perisai menggunakan modem radio M10 oleh Quectel. Hal ini

dimungkinkan untuk berkomunikasi dengan board menggunakan perintah AT. Perpustakaan *GSM* memiliki sejumlah besar metode untuk komunikasi dengan perisai. Perisai menggunakan pin digital 2 dan 3 untuk komunikasi serial perangkat lunak dengan M10. Pin 2 terhubung ke pin TX M10 dan pin 3 ke pin RX-nya. Lihat catatan ini untuk bekerja dengan Arduino Uno, Uno ADK, atau Leonardo. Pin PWRKEY modem terhubung ke pin Arduino 7. M10 adalah *modem Quad-band GSM / GPRS* yang bekerja pada frekuensi GSM850MHz, GSM900MHz, DCS1800MHz dan PCS1900MHz. Ini mendukung protokol TCP / UDP dan HTTP melalui koneksi GPRS. Kecepatan downlink data GPRS dan kecepatan transfer uplink maksimal adalah 85,6 kbps.Untuk antarmuka dengan jaringan selular, board memerlukan kartu SIM yang disediakan oleh operator jaringan. Lihat halaman awal untuk informasi tambahan tentang penggunaan SIM

2.3.5 *SMS (Short Massage Service)*

Teknologi telekomunikasi pada saat ini semakin berkembang, salah satu teknologi telekomunikasi yang sedang berkembang yaitu Short Massage *Service* atau biasa nya disebut dengan SMS. SMS adalah kemampuan untuk mengirim dan menerima pesan singkat dalam bentuk teks dari sebuah perangkat nirkabel, yaitu perangkat telekomunikasi telpon seluler, dalam hal ini perangkat nirkabel yang digunakan adalah telpon *seluler*. Teks tersebut bisa terdiri dari kata-kata atau nomor ataupun kombinasi *alphanumeric*. Pendapat lain mengenai pengertian SMS di utarakan oleh Romzi Imron (Romzi Imron 2004:1) yang mengungkapkan tentang pengertian SMS adalah sebagai berikut:

"Layanan yang banyak di aplikasikan pada jaringan komunikasi tanpa kabel yang memungkinkan dilakukan nya pengiriman pesan dalam bentuk *alphanumeric* antar terminal pelanggan (Ponsel) atau antara terminal pelanggan dengan sistem eksternal seperti *e-mail*, *paging*, *voice mail* dan sebagainya" (Imron,2004:1)

2.3.6 *Selenoid Door Lock*

Selenoid Door Lock adalah salah satu selenoid yang difungsikan khusus sebagai selenoid untuk pengunci pintu secara elektronik. Selenoid ini mempunyai dua

sistem kerja, yaitu Normaly Close (NC) dan Normaly Open (NO). Perbedaan dari keduanya adalah sebagai berikut ini:

Perbedaanya adalah jika cara kerja selenoid NC apabila diberi tegangan, maka selenoid akan memanjang (tertutup). Dan untuk cara kerja dari Selenoid NO adalah kebalikannya dari Selenoid NC. Biasanya kebanyakan *selenoid Door Lock* membutuhkan input atau tegangan kerja 12V DC tetapi ada juga *selenoid Door Lock* yang yang hanya membutuhkan input tegangan 5V DC dan sehingga dapat langsung bekerja dengan tegangan output dari pin IC digital. Namun jika anda menggunakan *Selenoid Door Lock* yang 12V DC. Berarti anda membutuhkan *power supply* 12V dan sebuah relay untuk mengaktifkannnya

Gambar 2.7 Selenoid Door lock

2.3.7 Mikrokontroller

Mikrocontroller adalah sebuah chip yang berfungsi sebagai pengontrol rangkaian elektronik dan umunya dapat menyimpan program pada umumnya terdiri dari CPU (*Central Processing Unit*), memori, I/O tertentu dan unit pendukung seperti *Analog-to-Digital Converter* (ADC) yang sudah terintegrasi di dalamnya. Kelebihan utama dari *Mikrokontroller* ialah tersedianya RAM dan peralatan I/O pendukung sehingga ukuran board *Mikrokontrolle*r menjadi sangat ringkas. (Arduino, 2016)

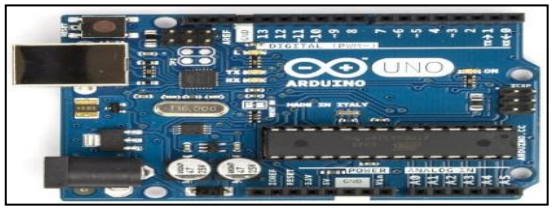
2.3.7.1 Modul Arduino Uno

Modul Arduino Uno adalah papan sirkuit berbasis Mikrokontroller ATmega328. IC (*integrated circuit*) ini memiliki 14 masukan/keluaran digital (6 keluaran untuk PWM), 6 analog masukan, resonator kristal keramik 16 MHz, Koneksi USB (*Universal Serial Bus*), soket adaptor, pin header ICSP, dan tombol *reset*. Hal inilah yang dibutuhkan untuk mensupport Mikrokontroller secara mudah

terhubung dengan kabel power USB atau kabel power supply adaptor AC ke DC atau juga battery (Arduino, 2016).

Arduino dikatakan sebagai sebuah platform dari physical computing yang bersifat open source. Arduino tidak hanya sekedar sebuah alat pengembangan, tetapi ia adalah

kombinasi dari hardware, bahasa pemrograman dan *Integrated Development Environment* (*IDE*) yang canggih. *IDE* adalah sebuah software yang sangat berperan untuk menulis program, meng-compile menjadi kode biner dan meng-upload ke dalam *memory microcontroller*. Ada banyak projek dan alat-alat dikembangkan oleh akademisi dan profesional dengan menggunakan arduino, selain itu juga ada banyak modul-modul pendukung (sensor, tampilan, penggerak dan sebagainya) yang dibuat oleh pihak lain untuk bisa disambungkan dengan Arduino. Arduino berevolusi menjadi sebuah platform karena ia menjadi pilihan dan acuan bagi banyak praktisi Bentuk fisik Arduino Uno seperti pada gambar 2.8

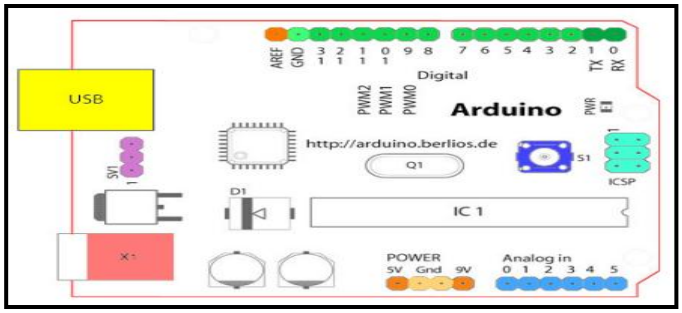


Gambar 2.8 Arduino Uno

(Sumber https://www.arduino.com,2016)

2.3.7.1.1 Blog Arduino Uno

Dengan mengambil contoh sebuah papan Arduino tipe USB, bagian-bagiannya dapat dijelaskan seperti gambar berikut :



Gambar 2.9 Blog Arduino Uno

(Sumber https://www.arduino.com,2016)

1. UART (*Universal Asynchronous Receiver/Transmitter*) adalah antar muka yang digunakan untuk komunikasi serial seperti pada RS-232, RS-422 dan RS-485.
2. 2KB RAM pada memory kerja bersifat volatile (hilang saat daya dimatikan), digunakan oleh variable-variabel di dalam program.
3. 32KB RAM flash memory bersifat non-volatile, digunakan untuk menyimpan program yang dimuat dari komputer. Selain program, flash memory juga menyimpan *bootloader*. *Bootloader* adalah program inisiasi yang ukurannya kecil, dijalankan oleh CPU saat daya dihidupkan. Setelah bootloader selesai dijalankan, berikutnya program di dalam RAM akan dieksekusi.
4. 1Kb eeprom bersifat non-volatile, digunakan untuk menyimpan data yang tidak boleh hilang saat daya dimatikan. Tidak digunakan pada papan Arduino.
5. CPU, bagian dari *Mikrokontroller* untuk menjalankan setiap instruksi dari program.
6. Port masukan/keluaran, pin-pin untuk menerima data digital atau analog, dan mengeluarkan data digital atau analog.
7. 14 pin masukan/keluaran digital (0-13)

   Berfungsi sebagai masukan atau keluaran, dapat diatur oleh program. Khusus untuk 6 buah pin 3, 5, 6, 9, 10 dan 11, dapat juga berfungsi sebagai pin analog keluaran dimana tegangan keluaran-nya dapat diatur. Nilai sebuah pin keluaran analog dapat diprogram antara 0 – 255, dimana hal itu mewakili nilai tegangan 0 – 5V.
8. USB Berfungsi untuk memuat program dari komputer ke dalam papan, memberi daya listrik kepada papan dan komunikasi serial antara papan dan komputer.
9. Sambungan SV1 Sambungan atau jumper untuk memilih sumber daya papan, apakah dari sumber eksternal atau menggunakan USB. Sambungan ini tidak diperlukan lagi pada papan Arduino versi terakhir karena pemilihan sumber daya eksternal atau USB dilakukan secara Otomatis.

10. Q1 – Kristal (*quartz crystal oscillator*) Jika *Mikrokontroller* dianggap sebagai sebuah otak, maka kristal adalah jantung-nya karena komponen ini menghasilkan detak-detak yang dikirim kepada *Mikrokontroller* agar melakukan sebuah operasi untuk setiap detak-nya. Kristal ini dipilih yang berdetak 16 juta kali per detik (16MHz).
11. Tombol Reset S1 Untuk me-reset papan sehingga program akan mulai lagi dari awal. Perhatikan bahwa tombol reset ini bukan untuk menghapus program atau mengosongkan *Mikrokontroller*.
12. *In-Circuit Serial Programming* (ICSP)Port ICSP memungkinkan pengguna untuk memprogram Mikrokontroller secara langsung, tanpa melalui *bootloader*. Umumnya pengguna Arduino tidak melakukan ini sehingga ICSP tidak terlalu dipakai walaupun disediakan.
13. IC 1 – *Mikrocontroller* Atmega Komponen utama dari papan Arduino, di dalamnya terdapat CPU, ROM dan RAM.
14. X1 – sumber daya eksternal Jika hendak disuplai dengan sumber daya eksternal, papan Arduino dapat diberikan tegangan DC antara 9-12V.
15. 6 pin masukan analog (0-5) Pin ini sangat berguna untuk membaca tegangan yang dihasilkan oleh sensor analog, seperti sensor suhu.

BAB III
METODOLOGI PENELITIAN

3.1 Alat Dan Bahan

3.1.1 Alat

Sebelum membuat Rancang Bangun Pengaman Pintu Rumah Otomatis Menggunakan E-KTP Berbasis Mikrokontroller ada beberapa peralatan yang harus disiapkan. Daftar peralatan yang digunakan dalam penelitian ini akan dituliskan pada Tabel 3.1.

Tabel 3.1 Alat Yang Dibutuhkan

-	Nama Alat	Spesifikasi	Fungsi	Jumlah
1	Laptop	Windows 7-10 32/64bit	Untuk membuat sebuah aplikasi yang akan di pakai di perangkat keras dan pernangkat lunak	1 unit
2	Multitester	Analog/Digital	digunakan untuk mengukur tegangan (ACV-DCV), dan kuat arus (mA-μA)	1 buah
3	Obeng	Obeng + dan -	Untuk merangkai alat	2 buah
4	Solder	-	Untuk menempelkan timah ke komponen	1 unit
5	Bor pcb	-	Untuk membuat lobang baut atau komponen	1 unit
6	Tang Potong	-	Untuk memotong kabel dan kaki komponen	1 buah
7	Kit Arduino	-	Komponen Komplit arduino UNO	1 unit
8	RFID Reader	-	Sebagai inputan untuk membaca E-KTP	1 unit
9	*Selenoid DoorLock*	-	Digunakan sebagai kunci pada pintu rumah	1 buah
10	*Relay*	-	Digunakan sebagai on/off Selenoid DoorLock	1 buah

11	*GSM Shield*	-	Digunakan untuk membrikan inormasi berupa pesan *SMS*	1 buah
12	Sensor Sentuh	-	Sebagai pembuka kunci pintu dari dalam	1 buah

3.1.2 Bahan

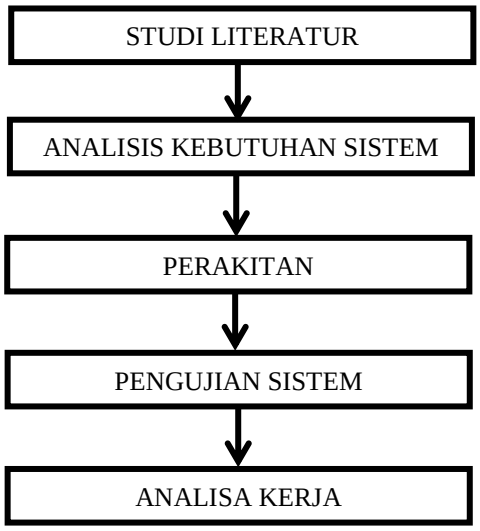
Sebelum membuat Rancang Bangun Pengaman Pintu Rumah Otomatis Menggunakan E-KTP Berbasis Mikrokontroller ada beberapa peralatan yang harus disiapkan. Daftar komponen yang digunakan dalam penelitian ini akan dituliskan pada Tabel 3.2.

Tabel 3.2 Bahan Yang Dibutuhkan

No	Nama Bahan	Sepesifikasi	Fungsi	Jumlah
1	E-KTP	-	Sebagai input yang akan digunakan pada *RFID*	3 buah
2	Kartu SIM	-	Digunakan untuk mengirim pesan berupa *SMS*	1
3	Pulsa	-	Sebagai pembayaran dalam SMS	RP. 5000

3.2 Tahapan Penelitian

Bab ini akan menjelaskan langkah-langkah penelitian yang akan dilakukan dalam Desain Sistem buka tutup gerbang dan pintu rumah otomatis. Alur penelitian yang digunakan seperti pada gambar 3.1



Gambar 3.1. Alur Penelitian

3.3 Penjelasan Alur Penelitian

1. **Studi Literatur**

   Mencari referensi dari berbagai sumber seperti halaman situs, jurnal, buku, dan lain sebagainya yang terkait dengan hasil penelitian yang akan dilakukan guna menambah pengetahuan peneliti dan informasi yang dapat digunakan untuk membantu proses pelaksanaan penelitian "Pengaman Pintu rumah Otomatis Menggunakan E-KTP".

2. **Analisis Kebutuhan Sistem**

   Semua kebutuhan yang akan digunakan dalam membuat Sistem Kunci Elektronik Menggunakan E-KTP ini dilakukan proses analasis kebutuhan sistem yang bertujuan agar semua kebutuhan yang akan dipakai nantinya sesuai dengan hasil yang akan dibuat

3. **Perakitan**

   Dengan kebutuhan yang telah dianalisis, mulai ke tahap perakitan pada tahap ini semua perancangan yang telah di buat kemudian akan dirakit dan coding yang

telah dibuat di-*compile* ke dalam sistem yang utuh dengan sumber tegangan, sensor, dan mikrokontroler-nya.

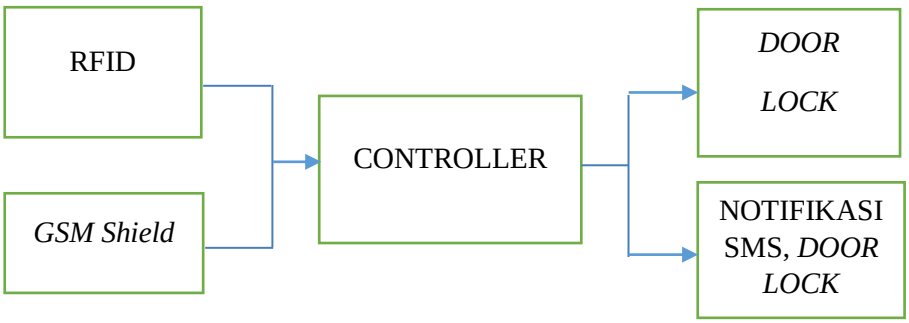
4. **Pengujian Sistem**

Setelah perakitan selesai, penulis akan melakukan pengujian sistem untuk menguji apakah sistem yang akan dirancang berjalan dengan baik dan sesuai tujuan awal sistem, serta untuk menetapkan hasil dan menemukan kesalahan-kesalahan yang mengganggu sistem untuk mencapai tujuan penelitian.

5. **Analisa Kerja**

Untuk analisa kerja, dilakukan bersama pada saat melakukan uji coba alat yang bertujuan untuk mengetahui kerja alat tersebut. Selain itu yang akan dianalisa adalah jarak, respon dalam untuk inputan pada sistem Pengaman Kunci Pintu Rumah Berbasis Mikrokontroller. Berdasarkan hasil pengujian sistem yang telah di dapat akan dianalisis untuk memastikan bahwa sistem yang telah dibuat sesuai dengan harapan

3.4 Analisa Perancangan Sistem



Gambar 3.2 Blok Diagram Sistem

Dari Gambar diatas dapat diketahui bahwa cara kerja Kunci Pintu Rumah Menggunakan *E-KTP* yang akan dibuat. Inputan dari sistem ini adalah *RFID* yang digunakan untuk membaca *E-KTP* dan sebuah *GSM Shield* yang terhubung ke Arduino. *RFID* berfungsi untuk membaca *E-KTP* yang di tempelkan pada *RFID* untuk membuka *Door* Lock, kemudian inputan yang kedua yaitu *GSM*

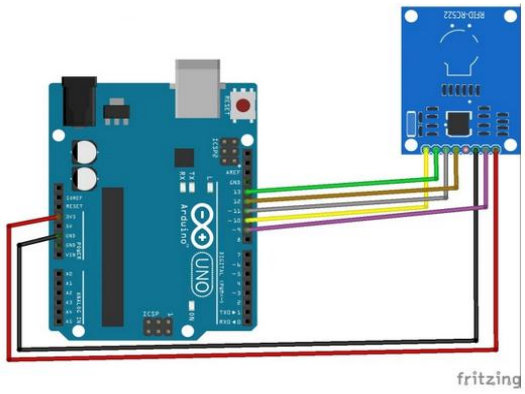
Shield berfungsi sebagai alternatif apabila hendak membuka pintu dari luar rumah namun kehilangan E-KTP nya dengan sebuah perintah yang dikirimkan ke *GSM Shield* melalaui SMS. Apabila E-KTP yang ditempelkan ke RFID benar, maka Door Lock akan terbuka dengan delay 5 detik untuk menutup kembali kunci secara otomatis, Apabila salah maka GSM Shield yang terhubung ke Arduino akan mengirimkan notifikasi berupa SMS ke *Handphone* pengguna. Outputan dari GSM Shield yang berisi perintah untuk mengontrol kunci pintu adalah Door Lock yang terbuka dengan delay 5 detik untuk menutup kembali kunci secara otomatis dan sebuah SMS sebagai notifikasi apabila kunci berhasil terbuka.

3.5 Perancangan Perangkat Keras

Perancangan menjadi bagian yang sangat penting dilakukan dalam pembuatan suatu alat karena dengan merancang terlebih dahulu komponen yang tepat akan mengurangi pengeluaran biaya berlebih. Untuk menghindari kerusakan komponen perlu dipahami karakteristik dari komponen-komponen tersebut.

3.5.1 Rangkaian RFID (*Radio Frequency Identification)*

Rangkaian RFID digunakan sebagai inputan untuk membuka kunci pintu yang akan diproses oleh arduino gambar rangkaian RFID dan tata letak dapat dilihat seperti pada gambar 3.3



Gambar 3.3 Rangkaian RFID (*Radio Frequency Identification)*

Pada rangkaian RFID hanya beberapa kaki yang dihubungkan ke pin digital arduino uno agar hasil proses pada arduino dapat memberikan outputan pembuka kunci pintu. Penggunaan PIN arduino uno dan *RFID* ditampilkan pada tabel 3.3

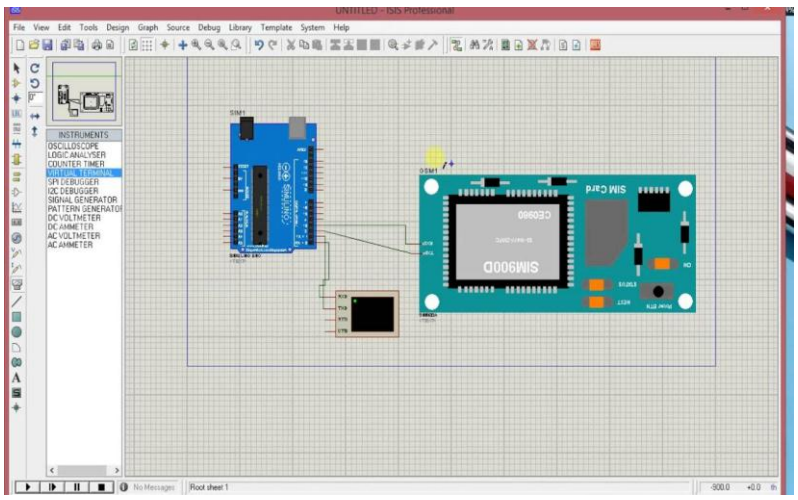
Tabel 3.3. Penggunaan Pin *RFID* ke Arduino Uno

Pin Arduino	**Keterangan**	**Pin *RFID***	**Keterangan**
10	Pin Input 10	SDA	Pin Output SDA
11	Pin Input 11	MOSI	Pin Output MOSI
12	Pin Input 12	MISO	Pin Output MISO
13	Pin Input 13	SCK	Pin Output SCK

Pada tabel rangkaian RFID dapat diketahui yaitu pin digital 10,11,12, dan 13 pada arduino akan dihubungkan ke pin SDA, SCK, MOSI, MISO pada pin RFID agar hasil proses pada arduino dapat membaca nomer ID pada E-KTP yang akan digunakan untuk membuka kunci pintu menggunakan Door Lock

3.5.2 Rangkaian GSM Shield

Rangkaian *GSM Shield* digunakan sebagai alat untuk mengirim notifikasi *SMS* dan menerima pesan *SMS* yang dikirimkan dari *Handphone* pemilik rumah untuk kontrol pembuka kunci pintu dengan perintah *SMS.* tata letak dapat dilihat seperti pada gambar 3.4



Gambar 3.4 Rangkaian GSM Shield

Pada rangkaian RFID hanya beberapa kaki yang dihubungkan ke pin digital arduino uno agar hasil proses pada arduino dapat memberikan outputan pembuka kunci pintu. Penggunaan PIN arduino uno dan *RFID* ditampilkan pada tabel 3.4

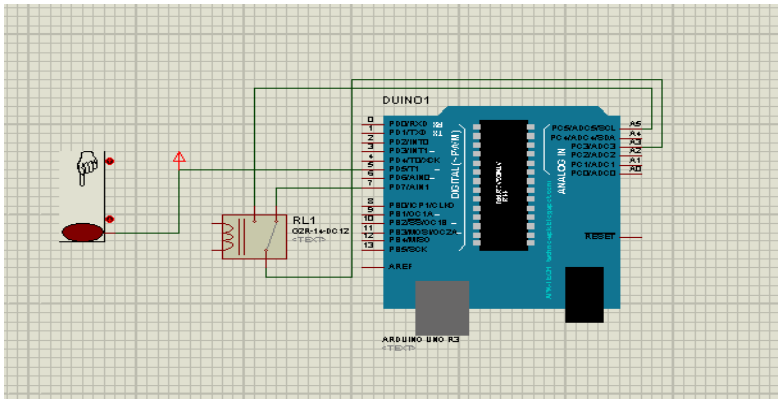
Tabel 3.4 Penggunaan pin Arduino ke *GSM Shield*

Pin Arduino	PIN GSM Shield	Keterangan
5V	VCC	Inputan Arus
GND	GND	Ground
7	RX	Receiver
8	TX	Transmitter

Pada tabel rangkaian GSM Shield dapat diketahui yaitu pin 5v, GND, 7, 8 pada Arduino akan dihubungkan pada pin VCC, GND, Rx, Tx agar hasil ketika scan E-KTP salah maka kaki pin 8 Arduino akan mengirim sinyal ke transmitter untuk diteruskan ke Handphone pemilik rumah dalam bentuk SMS.

3.5.3 Rangkaian Sensor sentuh

Rangkaian sensor sentuh digunakan apabila pemilik rumah hendak keluar namun pintu masih terkunci, Pemilik tinggal menyentuh sensor sentuh ini untuk membuka kunci nya tanpa harus *scan E-KTP* karena scan *E-KTP* hanya berlaku dari luar rumah. Berikut ini tata letak dapat dilihat seperti pada gambar 3.5



Gambar 3.5 Gambar rangkaian sensor sentuh

Pada rangkaian Sensor Sentuh hanya beberapa kaki yang dihubungkan ke pin arduino uno agar hasil proses pada arduino dapat memberikan outputan berupa pembuka kunci pintu. Penggunaan pin dapat dilihat pada tabel 3.5

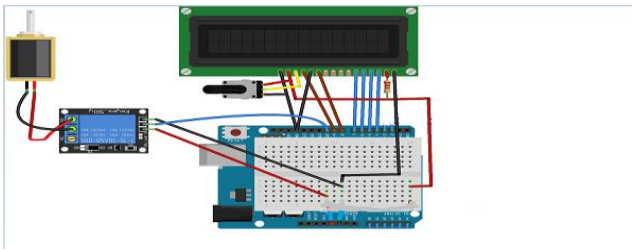
Tabel 3.5 Penggunaan pin Arduino ke Sensor Sentuh

Pin Arduino	PIN Sensor Sentuh	Keterangan
5V	VCC	Inputan Arus
GND	GND	Ground
5	OUT	Keluaran dari sensor sentuh diteruskan ke kaki 5 arduino

Pada tabel diatas dapat diketahui bahwa pin dari sensor sentuh yaitu VCC, GND, OUT dihubungkan ke Arduino pada pin 5v sebagai arus, Gnd, dan pin 5 arduino yang berfungsi untuk membuka Door Lock dari dalam rumah.

3.5.4 Rangkaian Door Lock

Rangkaian Door Lock digunakan untuk mengunci pintu rumah sebagai outputan dengan input berupa RFID yang digunakan untuk scan E-KTP, Kontrol Door Lock melalui SMS, dan sensor sentuh. Berikut ini tata letak dapat dilihat seperti pada gambar 3.6



Gambar 3.6 Gmbar rangkaian Door Lock

Pada rangkaian Door Lock hanya beberapa kaki yang dihubungkan ke pin arduino uno agar hasil proses pada arduino dapat memberikan outputan berupa pembuka kunci pintu. Penggunaan pin dapat dilihat pada tabel 3.6

Tabel 3.6 penggunaan pin Arduino ke Door Lock

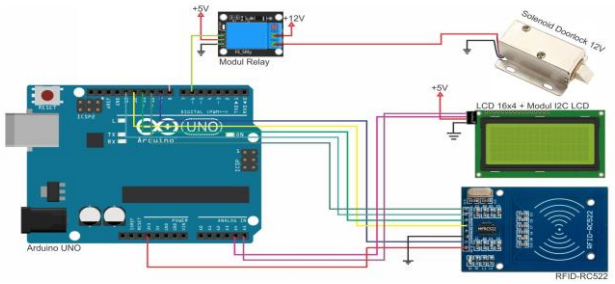
Pin Arduino	PIN Relay	Kaki Door Lock	Keterangan

5V	VCC	Vcc	Inputan arus
GND	GND	GND	Ground
4	In 1	-	-

Pada tabel diatas dapat diketahui bahwa pin Arduino 5v, GND, 4 terhubung ke pin relay VCC, GDN, IN 1 kemudian diteruskan ke kaki Door Lock VCC dan GND, dimana ketika Door Lock mendapat input, maka output akan mengirim sinyal ke In 1 melalui kaki 4 untuk mengaktifkan Door Lock.

3.5.5 Rangkaian Keseluruhan Sistem

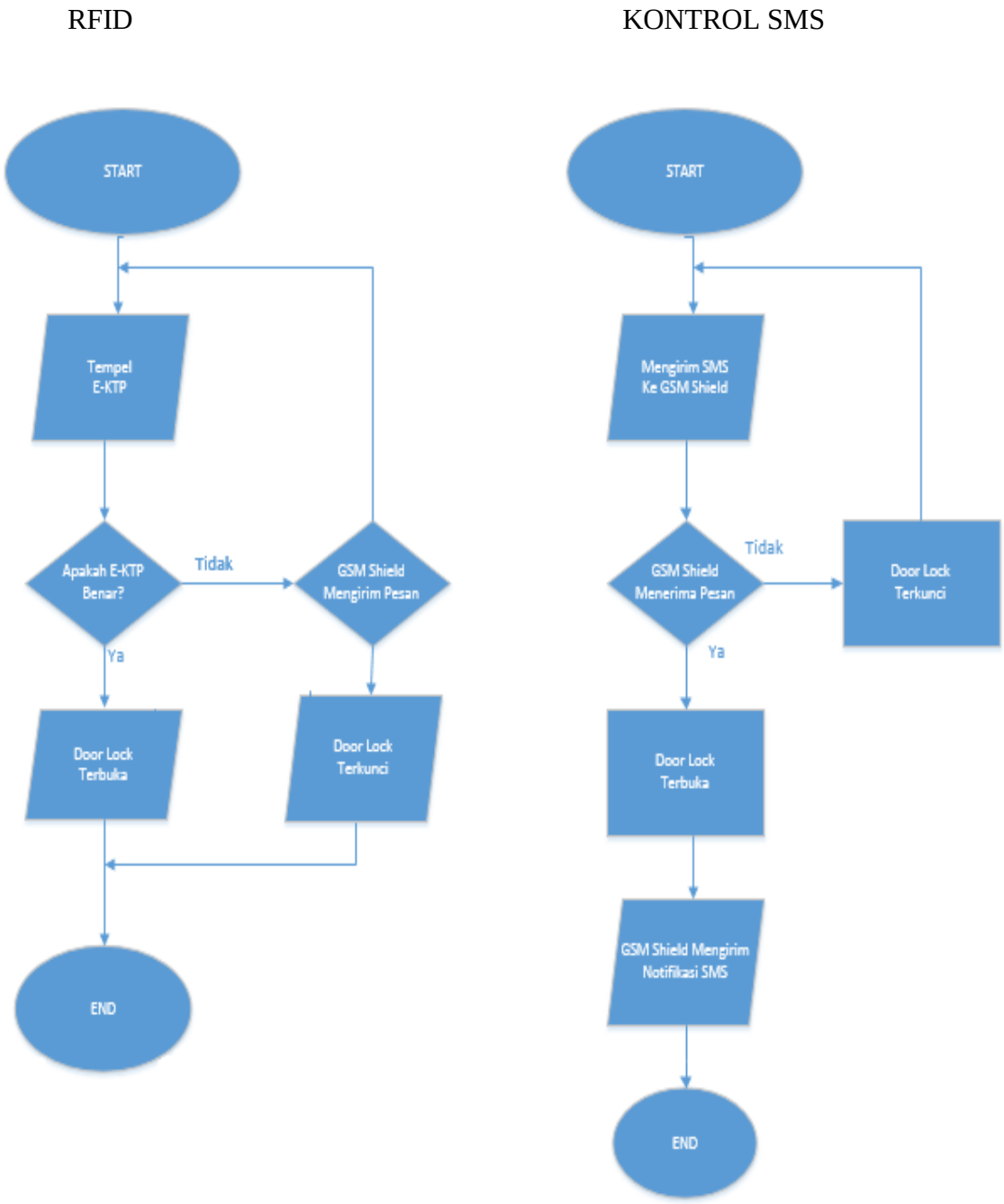
Pada rangkaian keseluruhan ini seperti gambar 3.9 dapat dijelaskan bahwa rangkaian keseluruhan yang terdiri dari RFID dan Arduino sebagai input yang berfungsi untuk membaca E-KTP yang ditempelkan ke RFID apabila benar maka Door Lock akan terbuka dan ketika E-KTP yang di scan ternyata salah maka otomatis GSM Shield akan mengirimkan notifikasi berupa SMS dan Door Lock tetap terkunci. Berikut ini tata letak dapat dilihat seperti pada gambar 3.7



Gambar 3.7 Rangkaian Keseluruhan Sistem

3.6 Perancangan Perangkat Lunak

Perancangan perangkat lunak dibuat dari pembuatan *flowchart* untuk pembuatan pada *hardware*. Pada gambar 3.8 akan ditampilkan *flowchart* dari program yang akan dibuat dalam penelitian ini



Gambar 3.8 *Flowchart* sistem.

3.7 Analisa Kebutuhan

Tahapan selanjutnya setelah membuat rancangan perangkat keras dan perangkat lunak yaitu membuat analisa kebutuhan sistem. Analisa ini dilakukan untuk

mengetahui alat dan komponen serta perangkat lunak apa saja yang akan digunakan untuk mengimplementasikan sistem.

3.8 Implementasi

Setelah mengumpulkan alat dan bahan, langkah selanjutnya adalah melakukan implementasi rancangan alat yang telah dibuat. Pada tahap ini hasil rancangan yang telah dibuat akan diimplementasikan untuk menjadi sistem yang sesungguhnya. Implementasi pada penelitian ini terbagi menjadi dua bagian, yaitu: Implementasi Hardware dan Implementasi Software. Implementasi Hardware merupakan tahap terakhir dari perancangan sistem yang dilakukan dalam tahap ini seluruh komponen dipasang sesuai dengan sistem yang telah dibuat.

3.8.1 Implementasi Perangkat Keras

Realisasi perangkat keras merupakan tahap terakhir dari perancangan yang telah dilakukan, Realisasi ini masih dalam bentuk Prototipe karna keterbatasan biaya. Dalam tahap ini seluruh komponen dipasang sesuai dengan sistem yang telah dibuat

3.8.2 Implementasi Perangkat Lunak

Penerapan perangkat lunak merupakan suatu tahap dimana program yang telah dirancang kemudian disimpan kedalam modul mikrokontroller melalui *downloader* dan menggunakan *software* sesuai dengan bahasa pemograman yang akan digunakan. Disini peneliti menggunakan bahasa C++ dan menggunakan *software* Arduino. Pada *Software* Arduino program ditulis kemudian di *compile*, tujuanya adalah untuk mengetahui apakah program yang dibuat sudah benar atau belum. Langkah terakhir yaitu meng-*upload kode* program kedalam modul mikrokontroller.

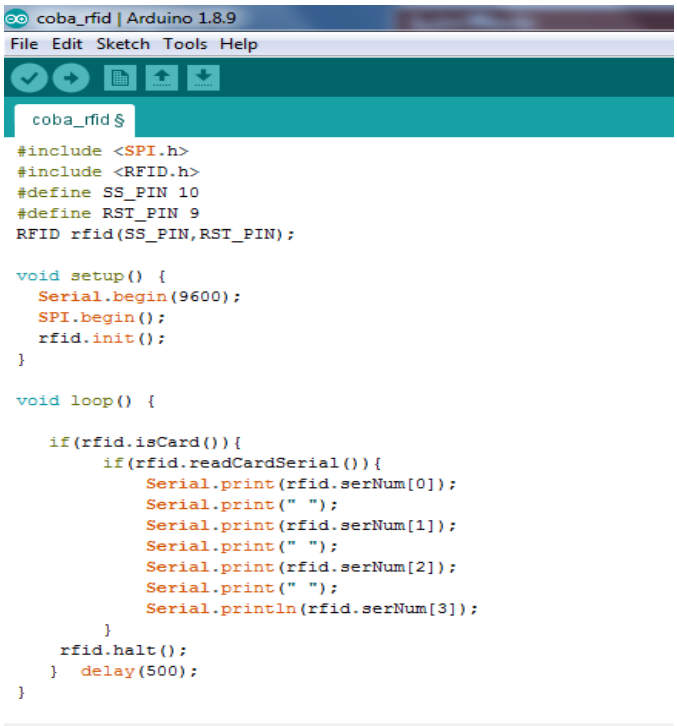
3.9 Pengujian Sistem

Setelah perancangan *hardware* dan *software* selesai, maka yang dilakukan adalah *running* program, pengujian tiap-tiap rangkaian apakah sudah sesuai dengan yang

diinginkan atau belum. Pengujian di lakukan pada bagian-bagian seperti pengujian respon, cakupan sistem, catu daya dan rangkaian keseluruhan pada sistem ini.

3.9.1 Pengujian RFID *Reader*

Rancangan pengujian RFID bertujuan untuk mengukur akurat respon ketika RFID E-KTP ditempelkan pada *reader* RFID dan peneliti akan menguji coba beberapa kali dengan menggunakan E-KTP yang berbeda apkah RFID dapat berkerja dengan baik. Dalam melakukan uji coba kali ini peneliti menggunakan *timer* yang digunakan sebagai pengukur lama respon RFID dalam membaca E-KTP yang digunakan sebagai pengganti ID card RFID. *Script* program arduino RFID dapat dilihat pada seperti berikut.

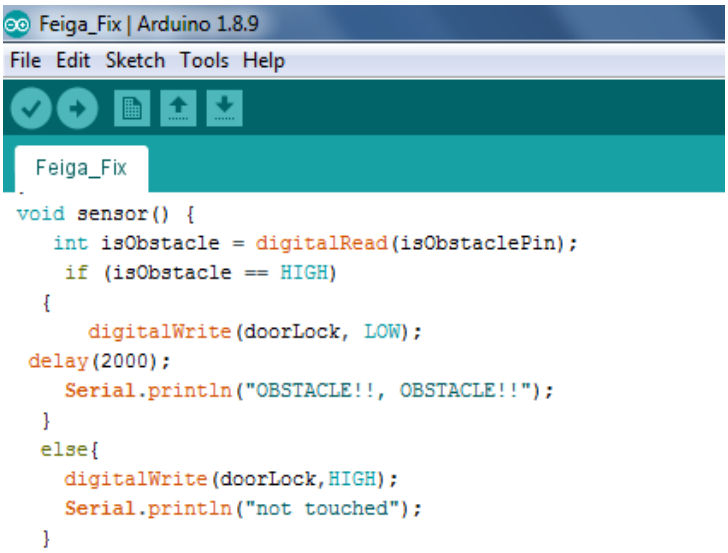


Gambar 3.9 program Arduino Untuk RFID

Pada pengujian RFID seperti gambar diatas, RFID yang digunakan hanya satu buah yang berfungsi sebagai pembaca E-KTP yang akan digunakan sebagai imput dari kunci elektronik pintu rumah.

3.9.2 Pengujian *Selenoid Door Lock*

Pengujian sensor ini bertujuan untuk mengetahui bagaimana *Door Lock* bekerja setelah mendapatkan sebuah input. *Script* program Arduino *Selenoid Door Lock* dapat dilihat pada seperti berikut



Gambar 3.10 Program Arduino untuk Door Lock

Pada pengujian *Door Lock* seperti gambar diatas, terlihat ketika *relay* bersatus *high*, maka *Door Lock* akan terbuka, apabila berstatus *low*, maka *Door Lock* akan tertutup secara otomatis.

3.9.3 Pengujian *GSM Shield*

Rancangan pengujian *gsm shield* bertujuan untuk mengetahui ketika *gsm shield* mendapat pintah dari inputan apakah dapat mengirimkan SMS kepada pemilik rumah dan mengukur berapa lama waktu respon *GSM Shield* dalam mengirimkan pesan SMS kepada pemilik rumah dalam melakukan ujicoba *GSM Shield* peneliti menggukan timer untuk mengukur waktu respon. *Script* program arduino RFID dapat dilihat pada seperti berikut.

Feiga_Fix | Arduino 1.8.9

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Feiga_Fix

```
void sendSMS(String message){
  // AT command to set SIM900 to SMS mode
  SIM900.print("AT+CMGF=1\r");
  delay(100);

  // REPLACE THE X's WITH THE RECIPIENT'S MOBILE NUMBER
  // USE INTERNATIONAL FORMAT CODE FOR MOBILE NUMBERS
  SIM900.println("AT + CMGS = \"+628996427315\"");
  delay(100);
  // Send the SMS
  SIM900.println(message);
  delay(100);

  // End AT command with a ^Z, ASCII code 26
  SIM900.println((char)26);
  delay(100);
  SIM900.println();
  // Give module time to send SMS
  delay(1000);
}
  void SendMessage1()
{
  Serial.println ("SIM900A Mengirim SMS");
 SIM900.println("AT+CMGF=1");    //Sets the GSM Module in Text Mode
  delay(1000);  // Delay of 1000 milli seconds or 1 second
  Serial.println ("Set SMS Number");
  SIM900.println("AT+CMGS=\"+628996427315\"\r"); // Replace with your mobile number
 delay(1000);
  Serial.println ("Set SMS Content");
```

Feiga_Fix | Arduino 1.8.9

File Edit Sketch Tools Help

Feiga_Fix§

```
  SIM900.println("AT+CMGS=\"+628996427315\"\r"); // Replace with your mobile number
 delay(1000);
  Serial.println ("Set SMS Content");
  SIM900.println("ADA MALING...");// The SMS text you want to send
  delay(100);
  Serial.println ("Finish");
 SIM900.println((char)26);// ASCII code of CTRL+Z
  delay(1000);
  Serial.println (" ->SMS Selesai dikirim");
}

void SendMessage2()
{
  Serial.println ("SIM900A Mengirim SMS");
 SIM900.println("AT+CMGF=1");    //Sets the GSM Module in Text Mode
  delay(1000);  // Delay of 1000 milli seconds or 1 second
  Serial.println ("Set SMS Number");
  SIM900.println("AT+CMGS=\"+628996427315\"\r"); // Replace with your mobile number
 delay(1000);
  Serial.println ("Set SMS Content");
  SIM900.println("PINTU TERBUKA.");// The SMS text you want to send
  delay(100);
  Serial.println ("Finish");
 SIM900.println((char)26);// ASCII code of CTRL+Z
  delay(1000);
  Serial.println (" ->SMS Selesai dikirim");
}
```

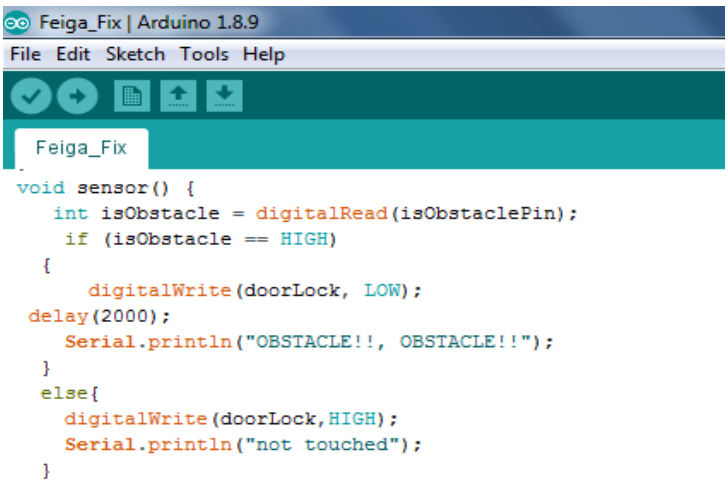
Gambar 3.11 Program *Arduino* Untuk *GSM shield*

Pada pengujian *GSM Shield* diatas, dapat terlihat pada bagian ("AT+CMGF=1"); ialah untuk menyetting mode SMS teks atau PDU (Program Data Unit), kemudian ada AT=CMGS yang berfungsi untuk mengirim SMS ke nomor yang telah ditentukan.

Apabila E-KTP yang ditempel pada RFID salah, maka GSM Shield akan mengirim SMS berupa notifikasi ke nomor yang tertera di kode program bertuliskan "ADA MALING…". Selanjutnya ketika hendak membuka kunci menggunakan SMS cukup ketik kan perintah "ON" kemudian kirimkan ke nomor yang ada pada GSM Shield untuk di teruskan perintahnya ke Arduino, berakhir dengan terbukanya Door Lock dan notifikasi SMS yang bertuliskan "Pintu Terbuka"

3.9.4 Pengujian Sensor Sentuh

Rancangan pengujian *Relay* bertujuan untuk mengetahui ketika *relay* diberikan status *HIGH* apakah *relay* dapat menghidupkan *Selenoid Door Lock* sesuai dengan program pada arduino. *Script* program arduino relay dapat dilihat pada seperti berikut



Gambar 3.12 kode program untuk sensor sentuh

Pada kode program pengujian sensor sentuh diatas. Dapat diketahui apabila sensor di sentuh, maka *relay* akan berstatus *high* yang kemudian berakhir dengan terbukanya Door Lock, apabila sensor tidak di sentuh maka akan bertatus *low* dan *Door Lock* akan kembali terkunci secara otomatis.

3.10 Analisa Kerja

Untuk analisa kerja, dilakukan bersama pada saat melakukan uji coba alat yang bertujuan untuk mengetahui kerja alat tersebut. Selain itu yang akan dianalisa adalah jarak, respon dalam untuk inputan pada sistem Pengaman Kunci Pintu Rumah Berbasis Mikrokontroller. Berdasarkan hasil pengujian sistem yang telah di dapat akan dianalisis untuk memastikan bahwa sistem yang telah dibuat sesuai dengan harapan

Tabel 3.7 Menguji RFID agar dapat men-scan E-KTP

Percobaan	Jarak	Hasil	Status Door Lock
1	2 cm	E-KTP Terbaca	Terbuka
2	5 cm	E-KTP Terbaca	Terbuka
3	7 cm	E-KTP Tidak Terbaca	Tertutup

Berdasarkan tabel diatas dapat dijelaskan bahwa RFID agar dapat berfungsi pada kunci elektronik pintu rumah maka E-KTP yang ditempelkan harus berjarak kurang dari 5 cm supaya terbaca oleh RFID

Tabel 3.8 Menguji *GSM Shield*

Percobaan	E-KTP yang di scan	Jumlah Salah	Hasil
1	Salah	1 kali	*GSM Shield* Mengirim SMS

Berdasarkan tabel diatas dapat disimpulkan bahwa ketika RFID membaca E-KTP yang salah sebanyak 1 kali, maka secara otomatis RFID mengirim pesan notifikasi berupa SMS.

BAB IV
HASIL DAN PEMBAHASAN

Bab ini berisi tentang hasil uji coba dan analisis terhadap sistem. Pengujian dimulai dengan memastikan setiap komponen (Arduino Uno, Sensor Touch, RFID, *Selenoid Door lock*, *Relay* dan *GSM Shield)* apakah alat yang dibuat dalam kondisi dapat bekerja dengan baik sesuai dengan program yang dibuat, kemudian mengecek setiap kabel yang terhubung dengan komponen yang digunakan telah terkoneksi, dimana rangkaiannya disesuaikan dengan gambar skematiknya. Pengujian yang dilakukan meliputi pengujian RFID, Selenoid Door Lock, *Relay*, *GSM Shield* dan pengujian sistem keseluruhan.

4.1 Hasil

Uji coba dilakukan untuk memastikan rangkaian yang dihasilkan mampu bekerja sesuai dengan yang diharapkan. maka terlebih dahulu dilakukan langkah pengujian dan mengamati langsung rangkaian serta komponen. Hasil pengukuran ini dapat diketahui rangkaian telah bekerja dengan baik atau tidak, sehingga apabila terdapat kesalahan dan kekurangan akan terdeteksi. Gambar 4.1 berikut ini merupakan gambar dari bentuk fisik alat yang telah dibuat.

Gambar. 4.1. Bentuk Fisik Alat

dari hasil perakitan peneliti mengetahui sistem kerja dari alat yang telah berkerja dengan baik yaitu. Pertama pemilik harus menempelkan E-KTP jika E-KTP yang ditempelkan benar maka *relay* akan berstatus *HIGH* yang digunakan untuk

mengaktifkan *Selenoid Door Lock*. Apabila E-KTP yang ditempel tidak sesuai dengan id yang terdaftar Maka secara otomatis GSM Shield akan mengirim notifikasi melalui SMS ke nomor yang ada pada Hp pemilik rumah. Kedua, ketika E-KTP hilang, pemilik masih tetap bisa membukanya dengan *control* menggunakan SMS dari HP pemilik dengan cara mengirim pesan ke nomor yang ada pada *GSM Shield*, dengan *delay* yang berfungsi untuk menutup *Door lock* secara otomatis, Ketiga Peneliti juga menambahkan Sensor *Touch* yang ditempatkan di dalam rumah untuk membuka *Door Lock* dari dalam tanpa Scan E-KTP, Karena Scan E-KTP hanya berlaku dari luar rumah.

4.1.1 Hasil Pengujian dan Pembahasan

Pada pengujian ini meliputi pungujian RFID, Sensor *Touch, Selenoid Door lock, Relay* dan *GSM Shield*. Pengujian ini dilakukan agar peneliti dapat mengetahui kelebihan dan kekurangan sistem yang telah di buat hasil pengujian sebagai berikut:

4.1.2 Pengujian Scan E-KTP

pengujian ini bertujuan untuk memastikan bahwa tidak ada kesalahan pada perintah terhadap keluaran yang didapatkan. Pada tahap ini peneliti melakukan pengujian dengan 4 kartu E-KTP yang berbeda agar dengan 3 E-KTP yang sudah terdaftar dalam program dan 1 yang belum terdaftar pengujian ini dilakukan agar peneliti dapat mengetahui jika nomer ID pada setiap E-KTP adalah berbeda :

Gambar 4.2 Pengujian Scan E-KTP

Tabel 4.1. Hasil Pengujian RFID

NO	Nomer E-KTP	Keterangan
1	13648363224	Akses Diterima
2	136469102175	Akses Diterima
3	1364107112151	Akses Diterima
4	Ktp selain yang terdaftar	Sistem Terkunci

4.1.3 Pengujian E-KTP untuk membuka *Door Lock*

Pada pengujian ini dilakukan untuk mengetahui apakah E-KTP dapat dengan baik dalam melakukan input untuk membuka *Door Lock*, hasil pengujian dapat dilihat seperti pada tabel 4.2.

Tabel 4.2. Hasil Pengujian *Relay*

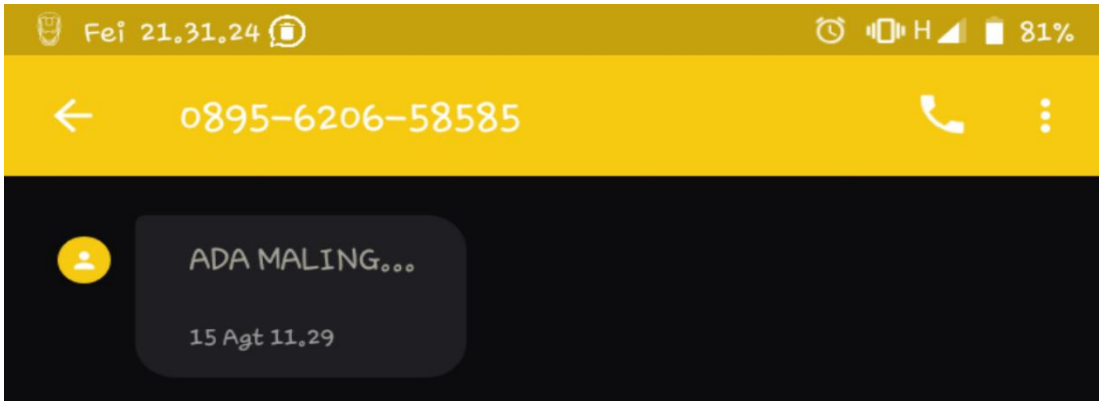
Nomor E-KTP	Status Door Lock	Status Relay	Keterangan
13648363224	Terbuka	HIGH	Door Lock terbuka
136469102175	Terbuka	HIGH	Door Lock terbuka
1364107112151	Terbuka	HIGH	Door Lock terbuka
Selain yang terdaftar	Tertutup	LOW	Door Lock tertutup, GSM Shield mengirimkan pesan

Dari hasil tabel diatas dapat diketahui yaitu pada ujicoba ke 1 sampai dengan ujicoba ke 3 dengan nomer E-KTP yang terdaftar maka dapat diketahui jika hanya melakukan 1 kali scan maka *relay* 1 akan HIGH untuk menyalakan Door Lock sedangan pada ujicoba ke 2 dengan nomor E-KTP tidak terdaftar maka GSM

Shield akan Otomatis mengirim pesan, ujicoba ke 3 dengan cara mengirim pesan berupa SMS ke GSM Shield untuk membuka Door Lock.

4.1.4 Hasil Pengujian *Gsm Shield*

pengujian ini bertujuan untuk memastikan bahwa jika scan E-KTP yang ditempelkan salah sebanyak 1 kali maka apakah GSM Shield dapat dengan baik salam mengirimkan SMS pengujian pada tahap ini akan ditampilkan pada gambar berikut :



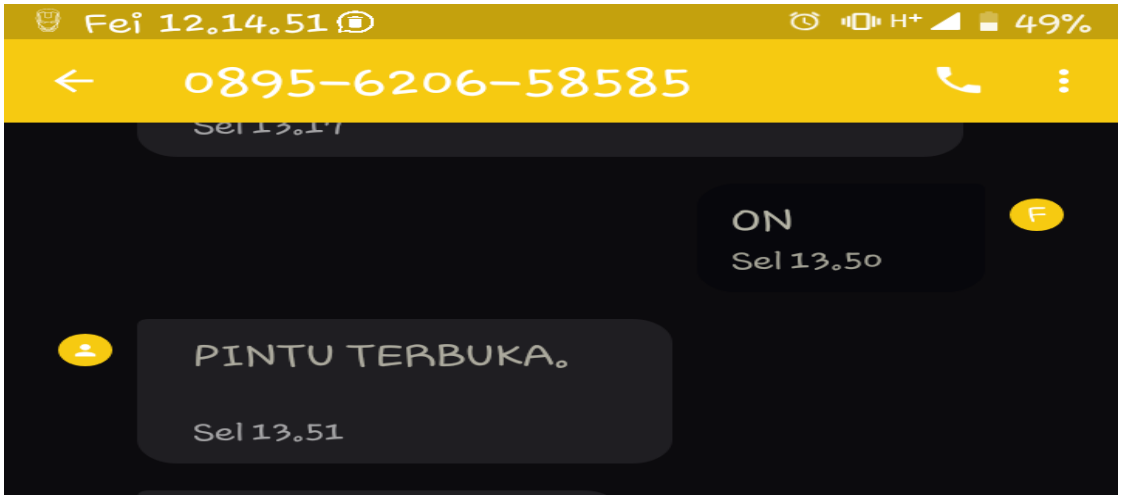
Gambar 4.3 Notifikasi Jika E-KTP tidak terdaftar ditempelkan ke RFID

Tabel 4.3. Hasil Pengujian *Gsm Shield*

Nomor E-KTP	Kesalahan Scan	Status GSM Shield	Waktu respon pengiriman sms
1234567	1 kali	*Gsm Shield* Mengirim SMS	5-10 detik
2134567	1 kali	*Gsm Shield* Mengirim SMS	5-10 detik

Tabel 4.4. Hasil Pengujian Kontrol *Door Lock* Menggunakan SMS

Nomor	Status *GSM Shield*	Status relay	keterangan	Status GSM Shield setelah kunci terbuka
08996427315	Menerima Pesan	High	Doorlock Terbuka	Mengirim Pesan



Gambar 4.4 Notifikasi Kontrol SMS

Dari hasil tabel diatas dapat diketahui yaitu pada uji coba ke 1 sampai dengan uji coba ke 2 dengan nomer E-KTP yang tidak terdaftar maka dapat diketahui jika kesalahan dalam melakukan scan sebanyak 1 kali maka *GSM Shield* akan mengirimkan SMS kepada pemilik rumah dan Door Lock tetap terkunci dan hasil pada tabel 4.5 dapat diketahui Doorlock dapat dikontrol menggunakan SMS dengan rentang waktu 5-10 detik seperti yang tertera pada Gambar 4.4

4.2 Pengujian Sistem Secara Keseluruhan

Pengujian sistem secara keseluruhan dilakukan untuk menguji kinerja Sistem Pengaman Pintu Rumah Menggunakan E-KTP Berbasis Mikrokontroler. Dari hasil ujicoba sistem dapat diketahui bahwa sistem dapat berkerja dengan baik sesuai perintah pada program yang telah dibuat dapat dilihat seperti pada tabel 4.5. berikut hasil pengujian sistem keseluruhan.

Tabel 4.5. Hasil Pengujian Sistem Keseluruhan

Nomor E-KTP	Jumlah Scan	Relay	Keterangan
13648363224	1 kali	HIGH	Door Lock terbuka
136469102175	1 kali	HIGH	Door Lock terbuka
1364107112151	1 kali	HIGH	Door Lock terbuka
Selain yang terdaftar	1 kali	LOW	Door Lock tertutup, GSM Shield mengirimkan pesan

Nomor	Status *GSM Shield*	Status *relay*	keterangan	Status *GSM Shield* setelah kunci terbuka
08996427315	Menerima Pesan	High	*Doorlock* Terbuka	Mengirim Pesan

Telah berhasil membuat alat Pengaman Pintu Rumah Menggunakan E-KTP Berbasis Mikrokontroler. jika hanya melakukan 1 kali scan maka relay 1 akan *HIGH* untuk menyalakan *Doorlock* sedangan pada ujicoba ke 2 melakukan 1 kali scan menggunakan E-KTP tidak terdaftar yang berarti GSM Shield akan mengirim pesan kepada pemilik berupa notifikasi SMS dan pada ujicoba ke 3 melakukan *control* menggunakan nomor HP pemilik, ke Nomor yang ada pada GSM Shield yang berisi perintah untuk membuka pintu dengan waktu paling lama 20 detik, setelah terbuka maka doorlock akan kembali menutup secara otomatis setelah 5 detik.

BAB V
KESIMPULAN DAN SARAN

5.1 Kesimpulan

Berdasarkan hasil pengujian dan pengukuran didapat kesimpulan sebagai berikut :

1. Pengaman Kunci Pintu Rumah Menggunakan E-KTP Berbasis Mikrokontroler ini setelah diuji, alat dapat berkerja dengan baik ketika mengirimkan notofikasi berupa SMS jika E-KTP tidak terdaftar.
2. GSM Shield dapat mengontrol Selenoid Dorr Lock untuk membuka kunci dengan cara mengirim SMS dari HP sang pemilik sebagai alternatif ketika pemilik rumah hendak masuk namun kehilangan E-KTP miliknya .
3. RFID RC522 yang digunakan dapat membaca atau mendeteksi nomer seri yang ada pada E-KTP dengan cukup baik.
4. Dari hasil ujicoba dapat diketahui jika gsm shield akan mengirimkan SMS apabila dalam melakukan scan E-KTP salah sebanyak 1 kali dengan jeda waktu 5-10 detik
5. Scan E-KTP hanya berlaku ketika pemilik rumah hendak masuk dari luar ke dalam rumah

5.2 Saran

Adapun saran yang dapat disampaikan penulis dari sistem pengaman Kunci Pintu Rumah Menggunakan E-KTP Berbasis Mikrokontroler yaitu :

1. Peneliti selajutnya dapat menambahkan Alarm instan apabila terjadi scan KTP yang tidak terdaftar berupa Sirine.

2. Untuk pengembangan lebih lanjut pada alat tersebut dapat ditambahkan aplikasi yang dapat memonitoring keadaan sekitar rumah khusunya pada bagian pintu.

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April 1999
Revised October 2005

LM7805 • LM7806 • LM7808 • LM7809 • LM7810 • LM7812 • LM7815 • LM7818 • LM7824 • LM7805A • LM7806A • LM7808A •LM7809A • LM7810A • LM7812A • LM7815A • LM7818A • LM7824A

3-Terminal 1A Positive Voltage Regulator (Preliminary)

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Ordering Code:

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	−40°C - +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C - +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

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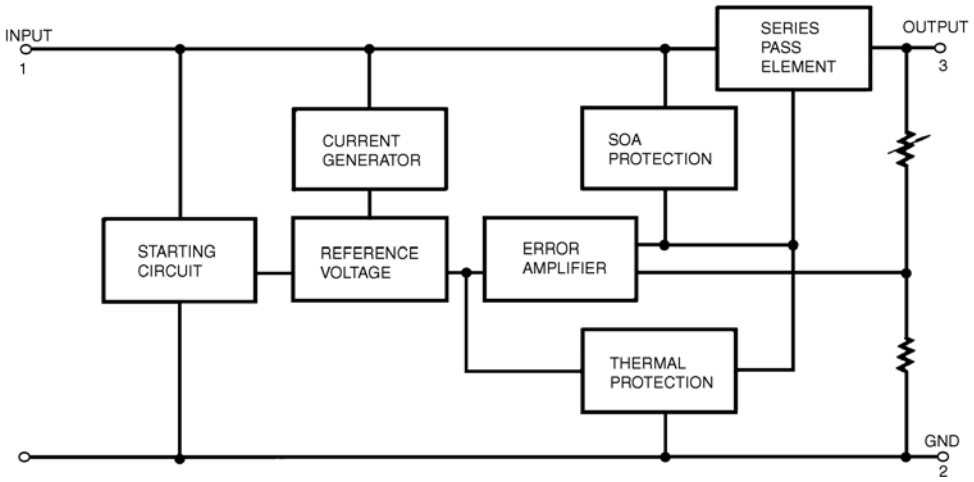
TO-220

Internal Block Diagram



Absolute Maximum Ratings(Note 1)

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V)	V_I	35	V
(for V_O = 24V)	V_I	40	V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	°C/W
Operating Temperature Range	T_{OPR}	0 ~ +125	°C
LM78xx		−40 ~ +125	°C
LM78xxA		0 ~ +125	°C
Storage Temperature Range	T_{STG}	−65 ~ +150	°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Electrical Characteristics (LM7805)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		4.8	5.0	5.2	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 7V to 20V		4.75	5.0	5.25	
Line Regulation	Regline	T_J = +25°C	V_O = 7V to 25V	–	4.0	100	mV
(Note 2)			V_I = 8V to 12V	–	1.6	50.0	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	9.0	100	mV
			I_O = 250mA to 750mA	–	4.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	0.03	0.5	mA
		V_I = 7V to 25V		–	0.3	1.3	
Output Voltage Drift (Note 3)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−0.8	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	42.0	–	μV/V_O
Ripple Rejection (Note 3)	RR	f = 120Hz, V_O = 8V to 18V		62.0	73.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 3)	rO	f = 1KHz		–	15.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	230	–	mA
Peak Current (Note 3)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 2: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 3: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7806)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 11V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		5.75	6.0	6.25	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 8.0V to 21V		5.7	6.0	6.3	
Line Regulation	Regline	T_J = +25°C	V_I = 8V to 25V	–	5.0	120	mV
(Note 4)			V_I = 9V to 13V	–	1.5	60.0	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	9.0	120	mV
(Note 4)			I_O = 250mA to 750mA	–	3.0	60.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 8V to 25V		–	–	1.3	
Output Voltage Drift (Note 5)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−0.8	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	45.0	–	μV/V_O
Ripple Rejection (Note 5)	RR	f = 120Hz, V_O = 8V to 18V		62.0	73.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 5)	rO	f = 1KHz		–	19.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 5)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 4: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 5: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7808)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 14V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		7.7	8.0	8.3	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 10.5V to 23V		7.6	8.0	8.4	
Line Regulation	Regline	T_J = +25°C	V_I = 10.5V to 25V	–	5.0	160	mV
(Note 6)			V_I = 11.5V to 17V	–	2.0	80.0	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	10.0	160	mV
(Note 6)			I_O = 250mA to 750mA	–	5.0	80.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	0.05	0.5	mA
		V_I = 10.5V to 25V		–	0.5	1.0	
Output Voltage Drift (Note 7)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−0.8	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	52.0	–	μV/V_O
Ripple Rejection (Note 7)	RR	f = 120Hz, V_O = 11.5V to 21.5V		56.0	73.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 7)	rO	f = 1KHz		–	17.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	230	–	mA
Peak Current (Note 7)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 6: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 7: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7809)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 15V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		8.65	9.0	9.35	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 11.5V to 24V		8.6	9.0	9.4	
Line Regulation	Regline	T_J = +25°C	V_I = 11.5V to 25V	–	6.0	180	mV
(Note 8)			V_I = 12V to 17V	–	2.0	90.0	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	12.0	180	mV
(Note 8)			I_O = 250mA to 750mA	–	4.0	90.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 11.5V to 26V		–	–	1.3	
Output Voltage Drift (Note 9)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	58.0	–	μV/V_O
Ripple Rejection (Note 9)	RR	f = 120Hz, V_O = 13V to 23V		56.0	71.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 9)	rO	f = 1KHz		–	17.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 9)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 8: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 9: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7810)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 16V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		9.6	10.0	10.4	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 12.5V to 25V		9.5	10.0	10.5	
Line Regulation	Regline	T_J = +25°C	V_I = 12.5V to 25V	–	10.0	200	mV
(Note 10)			V_I = 13V to 25V	–	3.0	100	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	12.0	200	mV
(Note 10)			I_O = 250mA to 750mA	–	4.0	400	
Quiescent Current	I_Q	T_J = +25°C		–	5.1	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 12.5V to 29V		–	–	1.0	
Output Voltage Drift (Note 11)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	58.0	–	μV/V_O
Ripple Rejection (Note 11)	RR	f = 120Hz, V_O = 13V to 23V		56.0	71.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 11)	rO	f = 1KHz		–	17.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 11)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 10: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 11: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7812)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 19V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		11.5	12.0	12.5	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 14.5V to 27V		11.4	12.0	12.6	
Line Regulation	Regline	T_J = +25°C	V_I = 14.5V to 30V	–	10.0	240	mV
(Note 12)			V_I = 16V to 22V	–	3.0	120	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	11.0	240	mV
(Note 12)			I_O = 250mA to 750mA	–	5.0	120	
Quiescent Current	I_Q	T_J = +25°C		–	5.1	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	0.1	0.5	mA
		V_I = 14.5V to 30V		–	0.5	1.0	
Output Voltage Drift (Note 13)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	76.0	–	μV/V_O
Ripple Rejection (Note 13)	RR	f = 120Hz, V_I = 15V to 25V		55.0	71.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 13)	rO	f = 1KHz		–	18.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	230	–	mA
Peak Current (Note 13)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 12: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 13: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7815)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 23V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		14.4	15.0	15.6	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 17.5V to 30V		14.25	15.0	15.75	
Line Regulation	Regline	T_J = +25°C	V_I = 17.5V to 30V	–	11.0	300	mV
(Note 14)			V_I = 20V to 26V	–	3.0	150	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	12.0	300	mV
(Note 14)			I_O = 250mA to 750mA	–	4.0	150	
Quiescent Current	I_Q	T_J = +25°C		–	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 17.5V to 30V		–	–	1.0	
Output Voltage Drift (Note 15)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	90.0	–	μV/V_O
Ripple Rejection (Note 15)	RR	f = 120Hz, V_I = 18.5V to 28.5V		54.0	70.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 15)	rO	f = 1KHz		–	19.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 15)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 14: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 15: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7818)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 27V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		17.3	18.0	18.7	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 21V to 33V		17.1	18.0	18.9	
Line Regulation	Regline	T_J = +25°C	V_I = 21V to 33V	–	15.0	360	mV
(Note 12)			V_I = 24V to 30V	–	5.0	180	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	15.0	360	mV
(Note 12)			I_O = 250mA to 750mA	–	5.0	180	
Quiescent Current	I_Q	T_J = +25°C		–	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 21V to 33V		–	–	1.0	
Output Voltage Drift (Note 17)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	110	–	μV/V_O
Ripple Rejection (Note 17)	RR	f = 120Hz, V_I = 22V to 32V		53.0	69.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 17)	rO	f = 1KHz		–	22.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 17)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 16: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 17: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7824)

(Refer to the test circuits. −40°C < T_J < 125°C, I_O = 500mA, V_I = 33V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		23.0	24.0	25.0	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 27V to 38V		22.8	24.0	25.25	
Line Regulation	Regline	T_J = +25°C	V_I = 27V to 38V	–	17.0	480	mV
(Note 18)			V_I = 30V to 36V	–	6.0	240	
Load Regulation	Regload	T_J = +25°C	I_O = 5mA to 1.5mA	–	15.0	480	mV
(Note 18)			I_O = 250mA to 750mA	–	5.0	240	
Quiescent Current	I_Q	T_J = +25°C		–	5.2	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	0.1	0.5	mA
		V_I = 27V to 38V		–	0.5	1.0	
Output Voltage Drift (Note 19)	$\Delta V_O/\Delta T$	I_O = 5mA		–	−1.5	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	60.0	–	μV/V_O
Ripple Rejection (Note 19)	RR	f = 120Hz, V_I = 28V to 38V		50.0	67.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 19)	rO	f = 1KHz		–	28.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	230	–	mA
Peak Current (Note 19)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 18: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 19: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7805A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 10V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		4.9	5.0	5.1	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 7.5V to 20V		4.8	5.0'	5.2	
Line Regulation	Regline	V_I = 7.5V to 25V, I_O = 500mA		–	5.0	50.0	mV
(Note 20)		V_I = 8V to 12V		–	3.0	50.0	
		T_J = +25°C	V_I = 7.3V to 20V	–	5.0	50.0	
			V_I = 8V to 12V	–	1.5	25.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	9.0	100	mV
(Note 20)		I_O = 5mA to 1mA		–	9.0	100	
		I_O = 250mA to 750mA		–	4.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 8V to 25V, I_O = 500mA		–	–	0.8	
		V_I = 7.5V to 20V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 21)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–0.8	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	µV/V_O
Ripple Rejection (Note 21)	RR	f = 120Hz, I_O = 500mA, V_I = 8V to 18V		–	68.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 21)	rO	f = 1KHz		–	17.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 21)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 20: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 21: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7806A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 11V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		5.58	6.0	6.12	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 8.6V to 21V		5.76	6.0	6.24	
Line Regulation	Regline	V_I = 8.6V to 25V, I_O = 500mA		–	5.0	60.0	mV
(Note 22)		V_I = 9V to 13V		–	3.0	60.0	
		T_J = +25°C	V_I = 8.3V to 21V	–	5.0	60.0	
			V_I = 9V to 13V	–	1.5	30.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	9.0	100	mV
(Note 22)		I_O = 5mA to 1mA		–	4.0	100	
		I_O = 250mA to 750mA		–	5.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	4.3	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 19V to 25V, I_O = 500mA		–	–	0.8	
		V_I = 8.5V to 21V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 23)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–0.8	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	µV/V_O
Ripple Rejection (Note 23)	RR	f = 120Hz, I_O = 500mA, V_I = 9V to 19V		–	65.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 23)	rO	f = 1KHz		–	17.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 23)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 22: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 23: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7808A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 14V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Output Voltage	V_O	T_J = +25°C		7.84	8.0	8.16	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 10.6V to 23V		7.7	8.0	8.3	
Line Regulation	Regline	V_I = 10.6V to 25V, I_O = 500mA		–	6.0	80.0	mV
(Note 24)		V_I = 11V to 17V		–	3.0	80.0	
		T_J = +25°C	V_I = 10.4V to 23V	–	6.0	80.0	
			V_I = 11V to 17V	–	2.0	40.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	12.0	100	mV
(Note 24)		I_O = 5mA to 1mA		–	12.0	100	
		I_O = 250mA to 750mA		–	5.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 11V to 25V, I_O = 500mA		–	–	0.8	
		V_I = 10.6V to 23V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 25)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–0.8	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	$\mu V/V_O$
Ripple Rejection (Note 25)	RR	f = 120Hz, I_O = 500mA, V_I = 11.5V to 21.5V		–	62.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 25)	rO	f = 1KHz		–	18.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 25)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 24: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 25: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7809A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 15V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output Voltage	V_O	T_J = +25°C		8.82	9.0	9.16	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 11.2V to 24V		8.65	9.0	9.35	
Line Regulation	Regline	V_I = 11.7V to 25V, I_O = 500mA		–	6.0	90.0	mV
(Note 26)		V_I = 12.5V to 19V		–	4.0	45.0	
		T_J = +25°C	V_I = 11.5V to 24V	–	6.0	90.0	
			V_I = 12.5V to 19V	–	2.0	45.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.0mA		–	12.0	100	mV
(Note 26)		I_O = 5mA to 1mA		–	12.0	100	
		I_O = 250mA to 750mA		–	5.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 12V to 25V, I_O = 500mA		–	–	0.8	
		V_I = 11.7V to 25V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 27)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	$\mu V/V_O$
Ripple Rejection (Note 27)	RR	f = 120Hz, I_O = 500mA, V_I = 12V to 22V		–	62.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 27)	rO	f = 1KHz		–	17.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 27)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 26: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 27: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7810A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 16V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output Voltage	V_O	T_J = +25°C		9.8	10.0	10.2	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 12.8V to 25V		9.6	10.0	10.4	
Line Regulation	Regline	V_I = 12.8V to 26V, I_O = 500mA		–	8.0	100	mV
(Note 28)		V_I = 13V to 20V		–	4.0	50.0	
		T_J = +25°C	V_I = 12.5V to 25V	–	8.0	100	
			V_I = 13V to 20V	–	3.0	50.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	12.0	100	mV
(Note 28)		I_O = 5mA to 1mA		–	12.0	100	
		I_O = 250mA to 750mA		–	5.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.0	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 12.8V to 25V, I_O = 500mA		–	–	0.8	
		V_I = 13V to 26V, T_J = +25°C		–	–	0.5	
Output Voltage Drift (Note 29)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	$\mu V/V_O$
Ripple Rejection (Note 29)	RR	f = 120Hz, I_O = 500mA, V_I = 14V to 24V		–	62.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 29)	rO	f = 1KHz		–	17.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 29)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 28: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 29: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7812A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 19V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output Voltage	V_O	T_J = +25°C		11.75	12.0	12.25	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 14.8V to 27V		11.5	12.0	12.5	
Line Regulation	Regline	V_I = 14.8V to 30V, I_O = 500mA		–	10.0	120	mV
(Note 30)		V_I = 16V to 22V		–	4.0	120	
		T_J = +25°C	V_I = 14.5V to 27V	–	10.0	120	
			V_I = 16V to 22V	–	3.0	60.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	12.0	100	mV
(Note 30)		I_O = 5mA to 1mA		–	12.0	100	
		I_O = 250mA to 750mA		–	5.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.1	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 14V to 27V, I_O = 500mA		–	–	0.8	
		V_I = 15V to 30V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 31)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	$\mu V/V_O$
Ripple Rejection (Note 31)	RR	f = 120Hz, I_O = 500mA, V_I = 14V to 24V		–	60.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 31)	rO	f = 1KHz		–	18.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 31)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 30: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 31: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7815A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 23V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output Voltage	V_O	T_J = +25°C		14.75	15.0	15.3	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 17.7V to 30V		14.4	15.0	15.6	
Line Regulation	Regline	V_I = 17.4V to 30V, I_O = 500mA		–	10.0	150	mV
(Note 32)		V_I = 20V to 26V		–	5.0	150	
		T_J = +25°C	V_I = 17.5V to 30V	–	11.0	150	
			V_I = 20V to 26V	–	3.0	75.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	12.0	100	mV
(Note 32)		I_O = 5mA to 1mA		–	12.0	100	
		I_O = 250mA to 750mA		–	5.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 17.5V to 30V, I_O = 500mA		–	–	0.8	
		V_I = 17.5V to 30V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 33)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	µV/V_O
Ripple Rejection (Note 33)	RR	f = 120Hz, I_O = 500mA, V_I = 18.5V to 28.5V		–	58.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 33)	rO	f = 1KHz		–	19.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 33)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 32: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 33: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7818A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 27V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output Voltage	V_O	T_J = +25°C		17.64	18.0	18.36	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 21V to 33V		17.3	18.0	18.7	
Line Regulation	Regline	V_I = 21V to 33V, I_O = 500mA		–	15.0	180	mV
(Note 34)		V_I = 21V to 33V		–	5.0	180	
		T_J = +25°C	V_I = 20.6V to 33V	–	15.0	180	
			V_I = 24V to 30V	–	5.0	90.0	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	15.0	100	mV
(Note 34)		I_O = 5mA to 1mA		–	15.0	100	
		I_O = 250mA to 750mA		–	7.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 12V to 33V, I_O = 500mA		–	–	0.8	
		V_I = 12V to 33V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 35)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–1.0	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	$\mu V/V_O$
Ripple Rejection (Note 35)	RR	f = 120Hz, I_O = 500mA, V_I = 22V to 32V		–	57.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 35)	rO	f = 1KHz		–	19.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 35)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 34: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 35: These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7824A)

(Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 33V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output Voltage	V_O	T_J = +25°C		23.5	24.0	24.5	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 27.3V to 38V		23.0	24.0	25.0	
Line Regulation	Regline	V_I = 27V to 38V, I_O = 500mA		–	18.0	240	mV
(Note 36)		V_I = 21V to 33V		–	6.0	240	
		T_J = +25°C	V_I = 26.7V to 38V	–	18.0	240	
			V_I = 30V to 36V	–	6.0	120	
Load Regulation	Regload	T_J = +25°C, I_O = 5mA to 1.5mA		–	15.0	100	mV
(Note 36)		I_O = 5mA to 1mA		–	15.0	100	
		I_O = 250mA to 750mA		–	7.0	50.0	
Quiescent Current	I_Q	T_J = +25°C		–	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 27.3V to 38V, I_O = 500mA		–	–	0.8	
		V_I = 27.3V to 38V, T_J = +25°C		–	–	0.8	
Output Voltage Drift (Note 37)	$\Delta V_O/\Delta T$	I_O = 5mA		–	–1.5	–	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A = +25°C		–	10.0	–	$\mu V/V_O$
Ripple Rejection (Note 37)	RR	f = 120Hz, I_O = 500mA, V_I = 28V to 38V		–	54.0	–	dB
Dropout Voltage	V_{DROP}	I_O = 1A, T_J = +25°C		–	2.0	–	V
Output Resistance (Note 37)	rO	f = 1KHz		–	20.0	–	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A = +25°C		–	250	–	mA
Peak Current (Note 37)	I_{PK}	T_J =+25°C		–	2.2	–	A

Note 36: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Note 37: These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

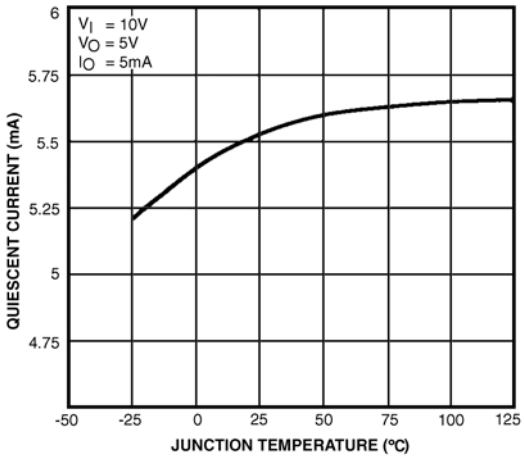


FIGURE 1. Quiescent Current

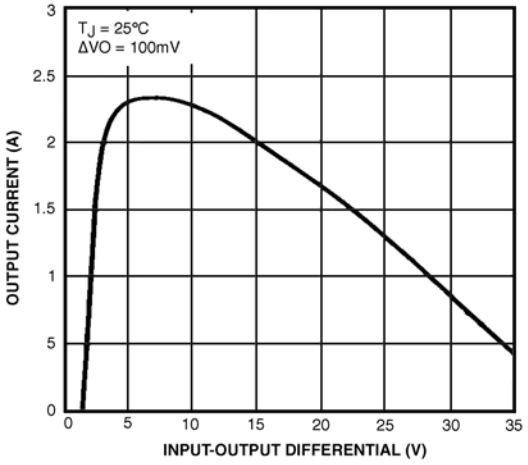


FIGURE 2. Peak Output Current

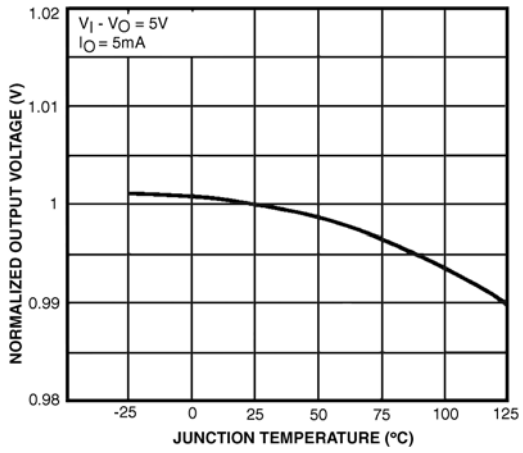


FIGURE 3. Output Voltage

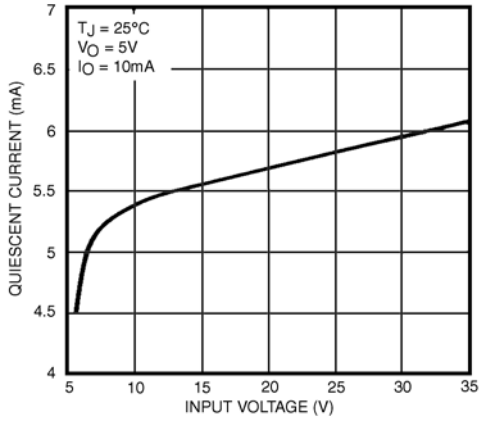


FIGURE 4. Quiescent Current

Typical Applications

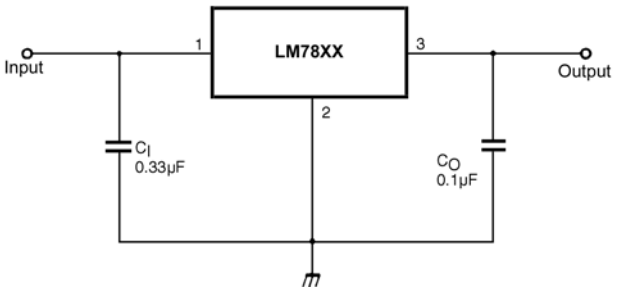


FIGURE 5. DC Parameters

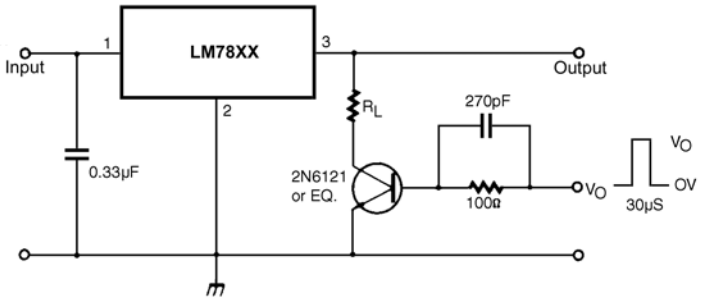


FIGURE 6. Load Regulation

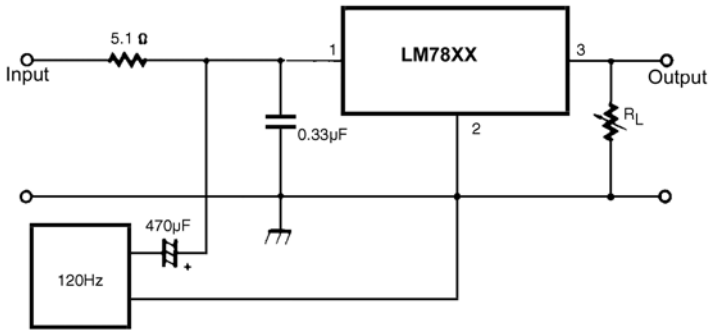


FIGURE 7. Ripple Rejection

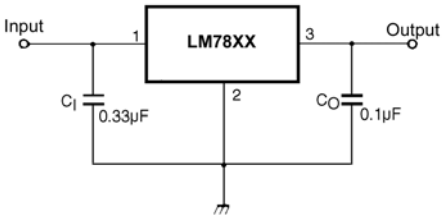
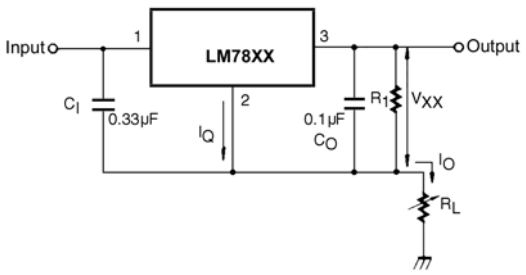


FIGURE 8. Fixed Output Regulator

Typical Applications (continued)



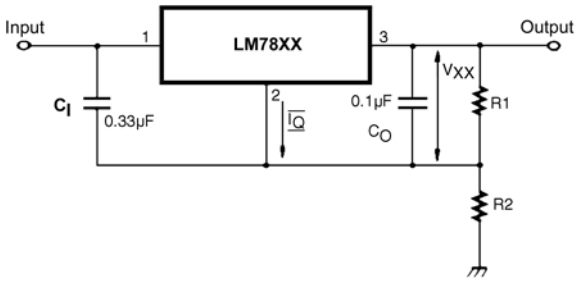
$$I_O = \frac{V_{XX}}{R_1} + I_Q$$

FIGURE 9.

Note: To specify an output voltage, substitute voltage value for "XX". A common ground is required between the Input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

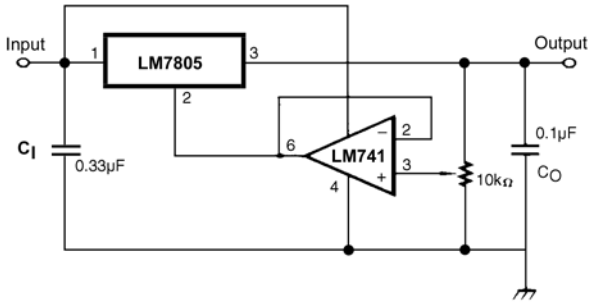
Note: C_I is required if regulator is located an appreciable distance from the power supply filter.

Note: C_O improves stability and transient response.



$$I_{RI} \geq 5\, I_Q$$
$$V_O = V_{XX}\,(1\, R_2 / R_1) + I_Q\, R_2$$

FIGURE 10. Circuit for Increasing Output Voltage



$$I_{RI} \geq 5\, I_Q$$
$$V_O = V_{XX}\,(1\, R_2 / R_1) + I_Q\, R_2$$

FIGURE 11. Adjustable Output Regulator (7V to 30V)

Typical Applications (continued)

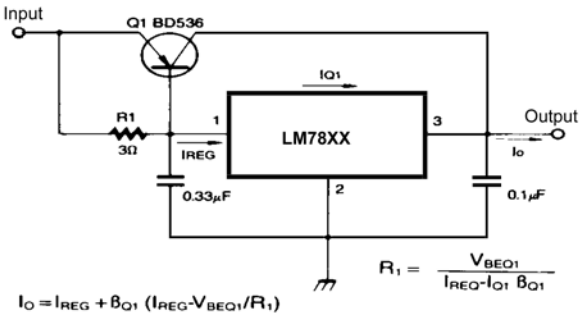


FIGURE 12. High Current Voltage Regulator

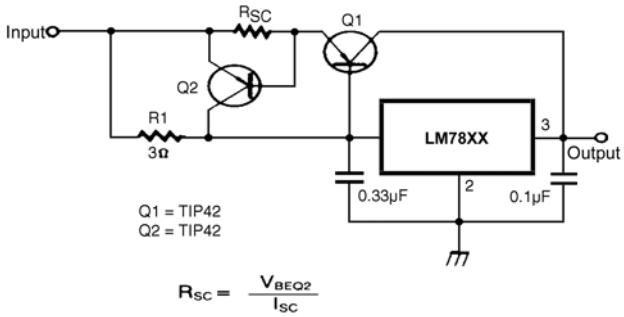


FIGURE 13. High Output Current with Short Circuit Protection

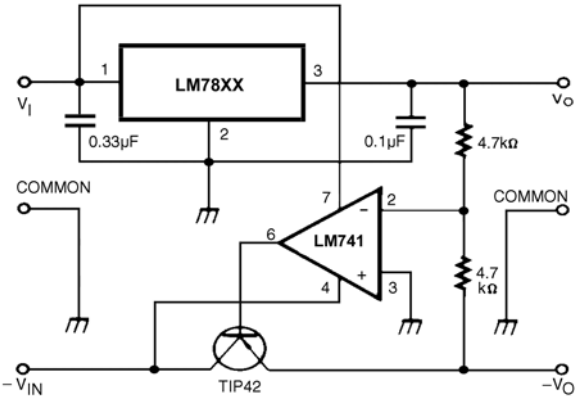


FIGURE 14. Tracking Voltage Regulator

Typical Applications (continued)

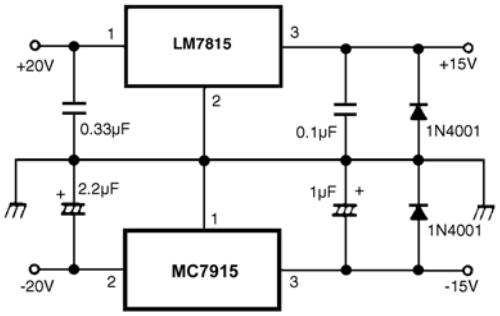


FIGURE 15. Split Power Supply (±15V - 1A)

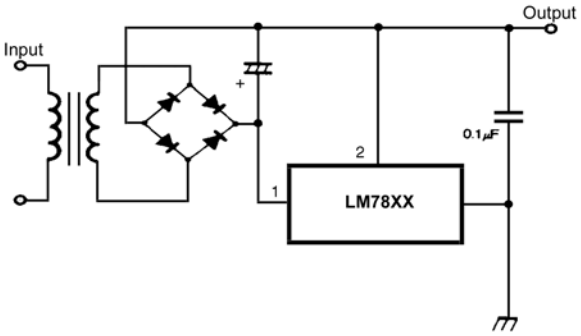


FIGURE 16. Negative Output Voltage Circuit

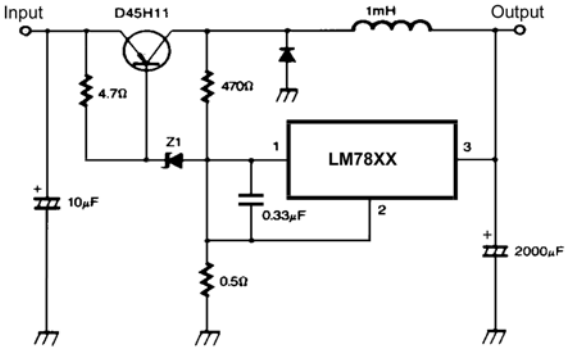
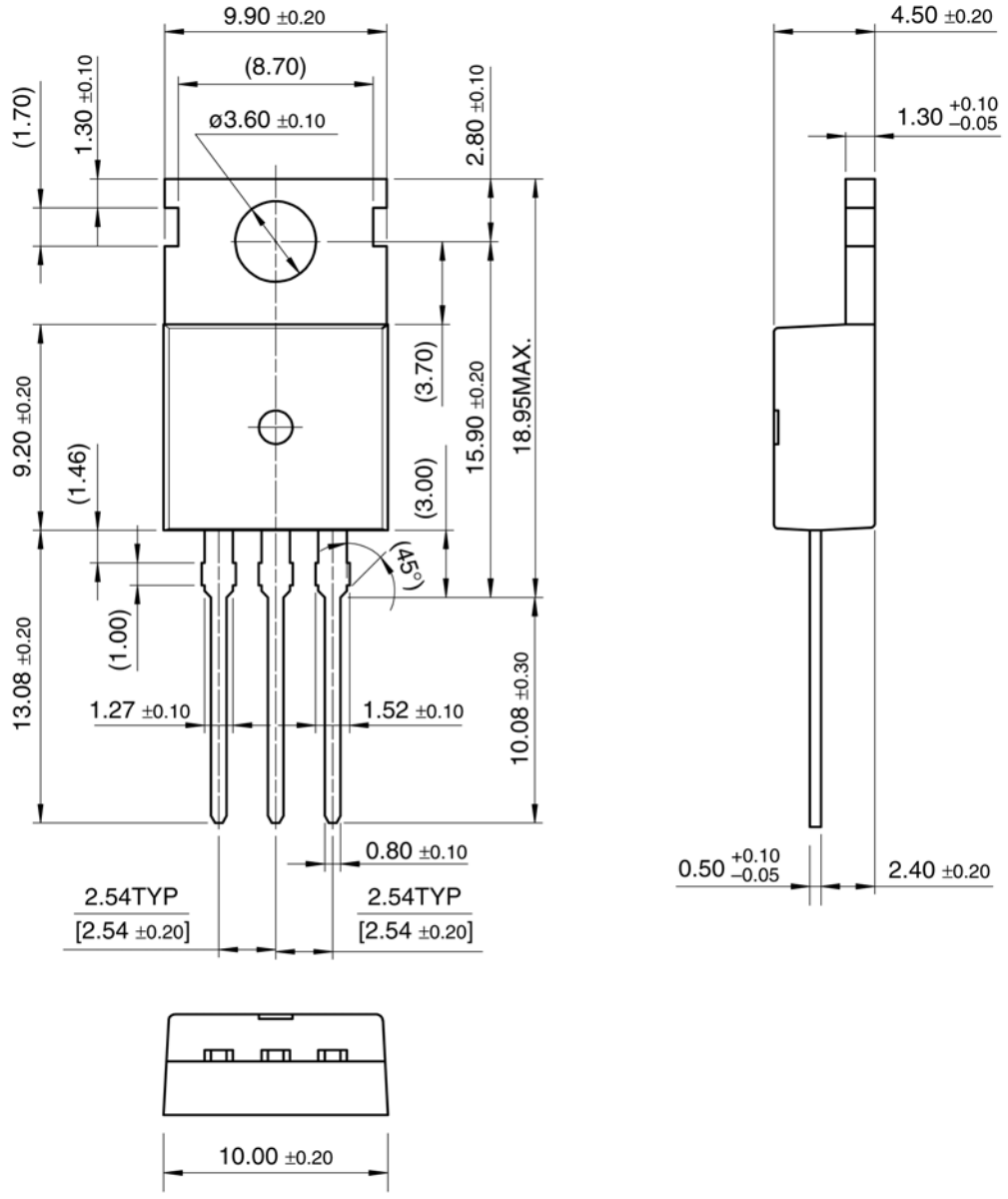


FIGURE 17. Switching Regulator

Physical Dimensions inches (millimeters) unless otherwise noted

TO-220



Package Number TO-220

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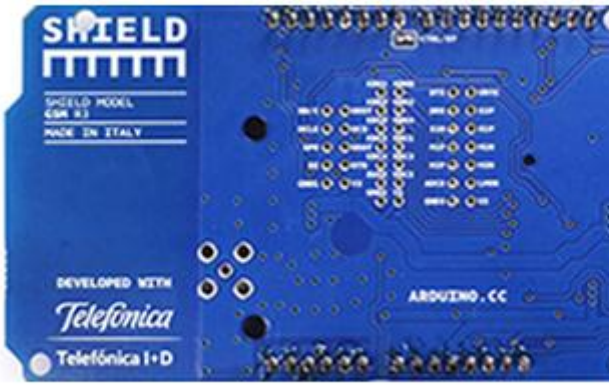
Definition of terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Arduino GSM Shield

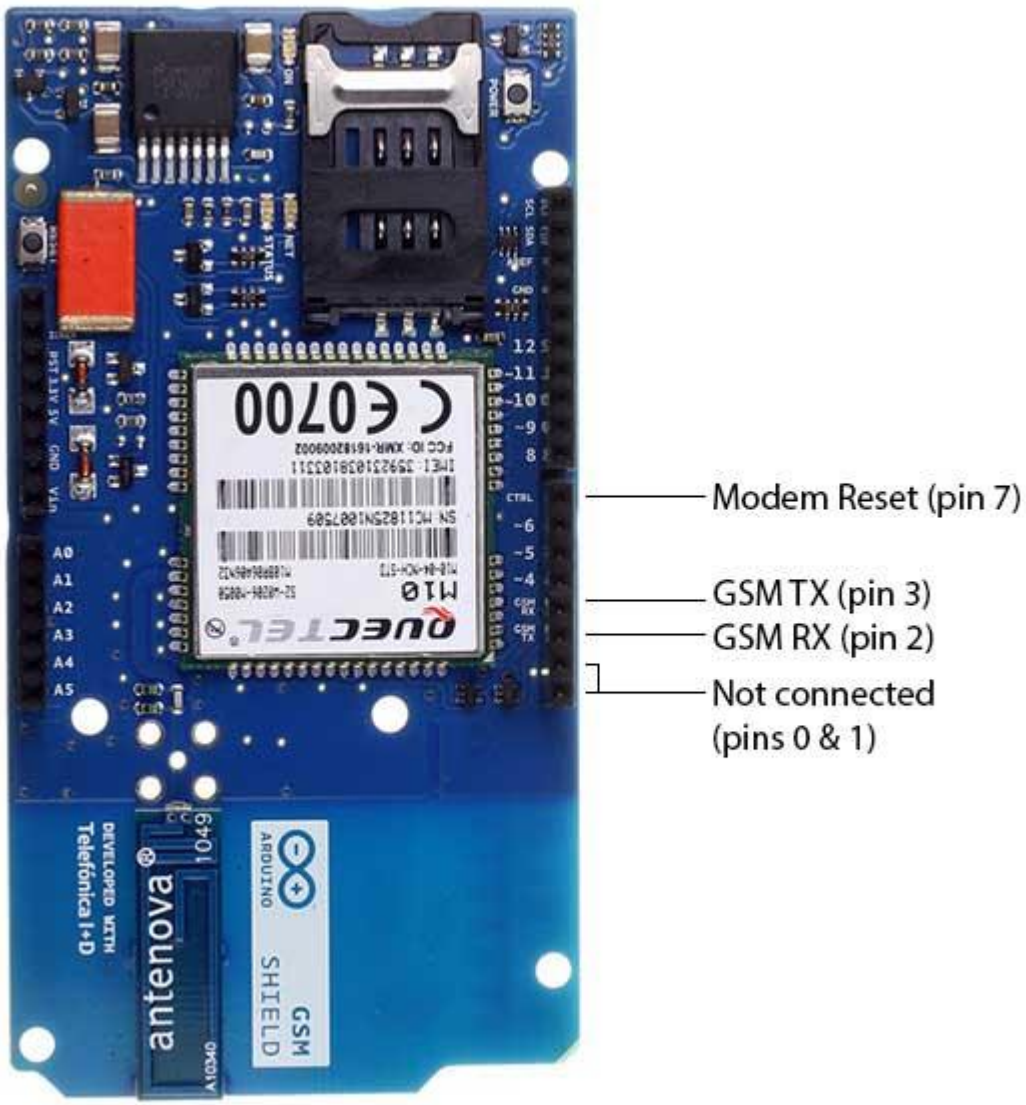


Arduino GSM Shield Front *Arduino GSM Shield Back*

Download: PDF of GSM shield schematic, Reference design
The GSM library is included with Arduino IDE 1.0.4 and later.

Overview

The Arduino GSM Shield connects your Arduino to the internet using the GPRS wireless network. Just plug this module onto your Arduino board, plug in a SIM card from an operator offering GPRS coverage and follow a few simple instructions to start controlling your world through the internet. You can also make/receive voice calls (you will need an external speaker and microphone circuit) and send/receive SMS messages.
As always with Arduino, every element of the platform – hardware, software and documentation – is freely available and open-source. This means you can learn exactly how it's made and use its design as the starting point for your own circuits. Hundreds of thousands of Arduino boards are already fueling people’s creativity all over the world, everyday. Join us now, Arduino is you!



- Requires and Arduino board (not included)
- Operating voltage 5V (supplied from the Arduino Board)
- Connection with Arduino Uno on pins 2, 3 (Software Serial) and 7 (reset).See these notes for working with a Mega, Mega ADK, or Leonardo.

Description

The Arduino GSM Shield allows an Arduino board to connect to the internet, make/receive voice calls and send/receive SMS messages. The shield uses a radio modem M10 by Quectel (datasheet). It is possible to communicate with the board using AT commands. The GSM library has a large number of methods for communication with the shield.
The shield uses digital pins 2 and 3 for software serial communication with the M10. Pin 2 is connected to the M10's TX pin and pin 3 to its RX pin. See these notes for working with an Arduino Mega, Mega ADK, or Leonardo. The modem's PWRKEY pin is connected to Arduino pin 7.
The M10 is a Quad-band GSM/GPRS modem that works at frequencies GSM850MHz, GSM900MHz, DCS1800MHz and PCS1900MHz. It supports TCP/UDP and HTTP protocols through a GPRS connection. GPRS data downlink and uplink transfer speed maximum is 85.6 kbps.
To interface with the cellular network, the board requires a SIM card provided by a network operator. See the getting started page for additional information on SIM usage.
The most recent revision of the board uses the 1.0 pinout on rev 3 of the Arduino Uno board.

Notes on the Telefonica/Bluevia SIM included with the shield

The GSM shield comes bundled with a SIM from Telefonica/Bluevia that will work well for developing machine to machine (M2M) applications. It is not necessary to use this specific card with the shield. You may use any SIM that works on a network in your area.
The Bluevia SIM card includes a roaming plan. It can be used on any supported GSM network. There is coverage throughout the Americas and Europe for this SIM, check the Bluevia service availability page for specific countries that have supported networks.
Activation of the SIM is handled by Bluevia. Detailed instructions on how to register and activate your SIM online and add credit are included on a small pamphlet that comes with your shield. The SIM must be inserted into a powered GSM shield that is mounted on an Arduino for activation.
These SIM card come without a PIN, but it is possible to set one using the GSM library's GSMPIN class.
You cannot use the included SIM to place or receive voice calls.
You can only place and receive SMS with other SIMs on the Bluevia network.
It's not possible to create a server that accepts incoming requests from the public internet. However, the Bluevia SIM will accept incoming requests from other SIM cards on the Bluevia network.
For using the voice, and other functions of the shield, you'll need to find a different network provider and SIM. Operators will have different policies for their SIM cards, check with them directly to determine what types of connections are supported.

Power requirements

It is recommended that the board be powered with an external power supply that can provide between 700mA and 1000mA. Powering an Arduino and the GSM shield from a USB connection is not recommended, as USB cannot provide the required current for when the modem is in heavy use.
The modem can pull up to 2A of current at peak usage, which can occur during data transmission. This current is provided through the large orange capacitor on the board's surface.

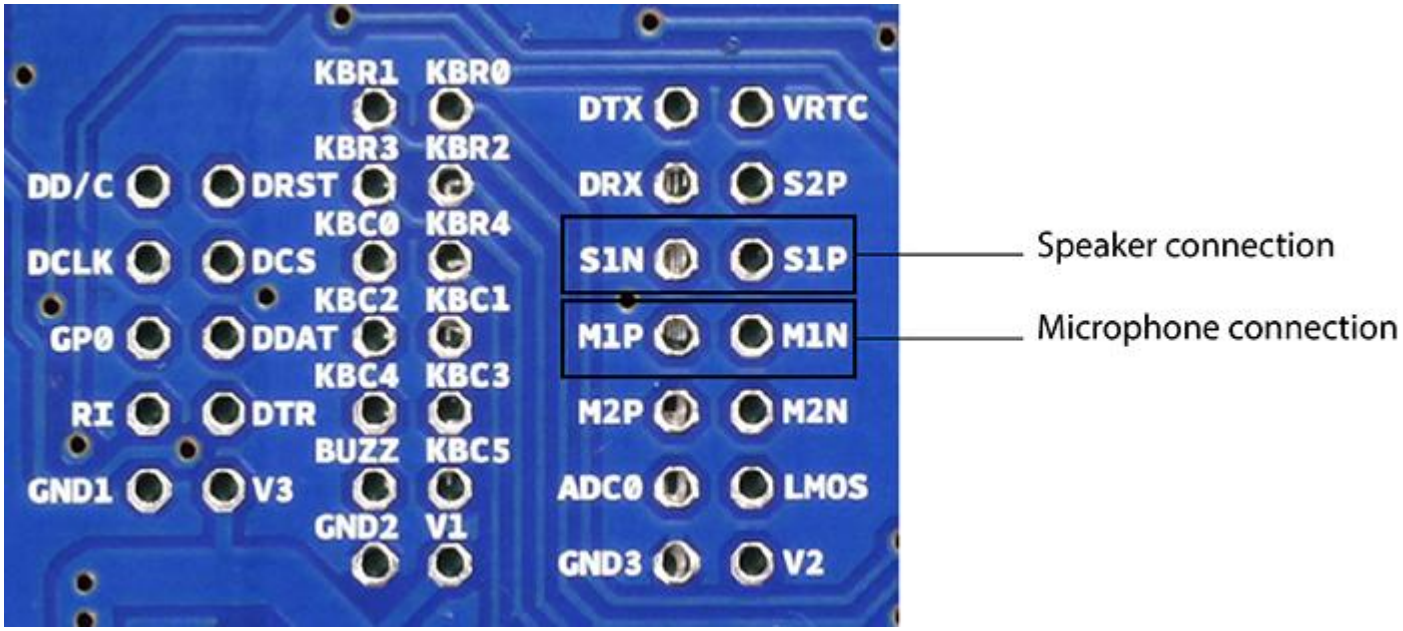
On board indicators

The shield contains a number of status LEDs:

- On: shows the Shield gets power.
- Status: turns on to when the modem is powered and data is being transferred to/from the GSM/GPRS network.
- Net: blinks when the modem is communicating with the radio network.

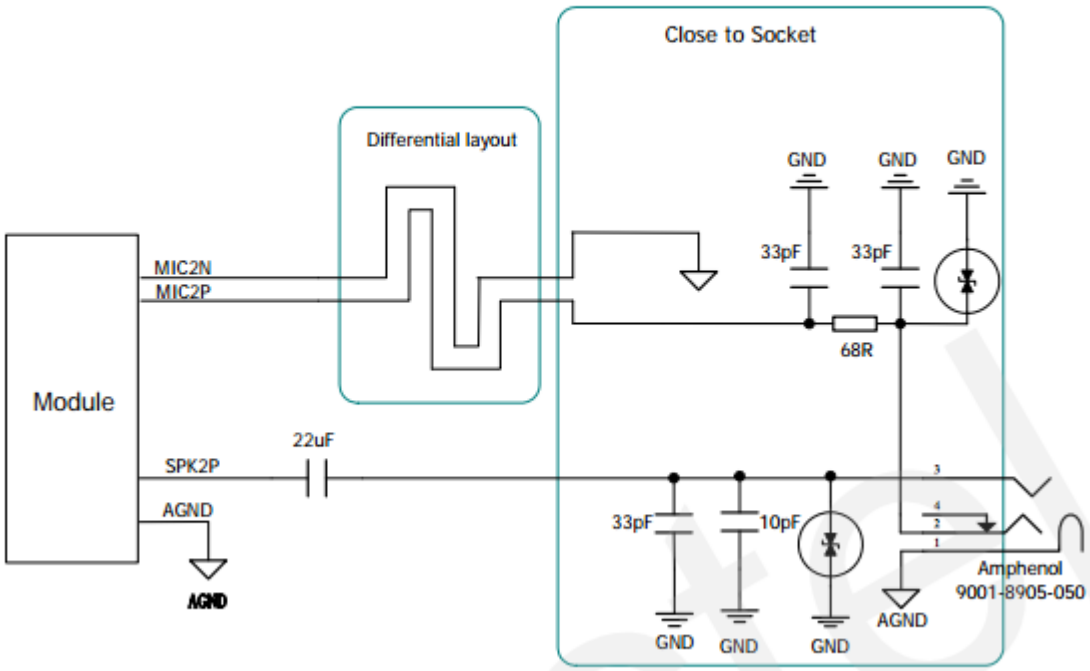
On board interfaces

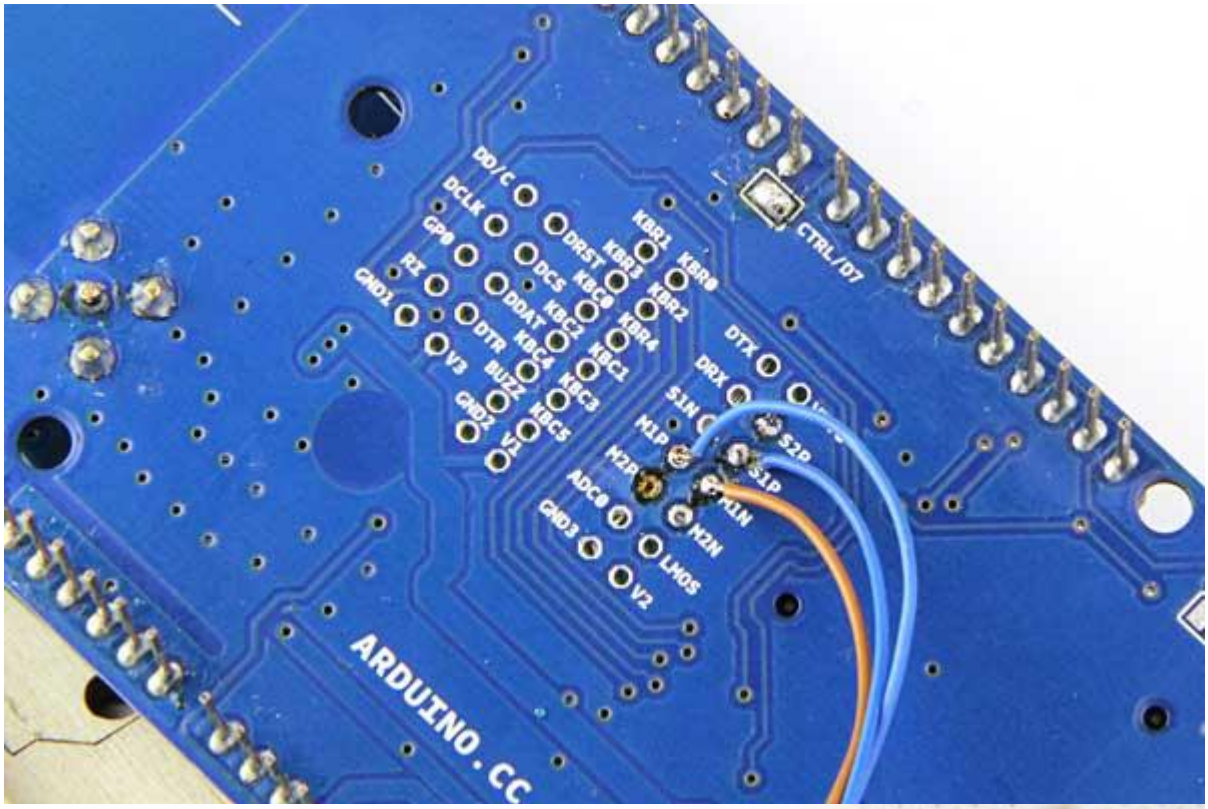
The shield supports AIN1 and AOUT1 as audio interfaces; an analog input channel and an analog output channel. The input, exposed on pins MIC1P/MIC1N, can be used for both microphone and line inputs. An electret microphone can be used for this interface. The output, exposed as lines SPK1P/SPK1N, can be used with either a receiver or speaker. Through the modem, it is possible to make voice calls. In order to speak to and hear the other party, you will need to add a speaker and microphone.

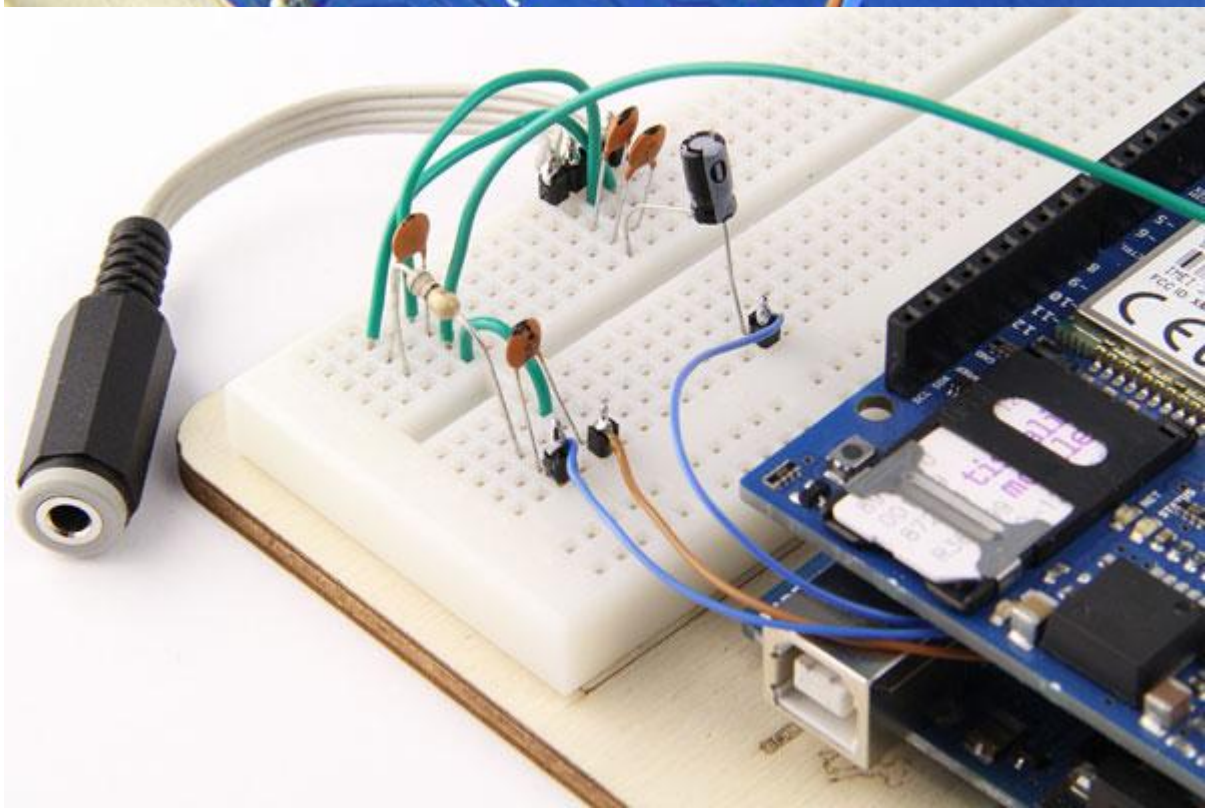


On page 43 of the modem documentation, there is an example voice and sound circuit that will connect to an earphone:

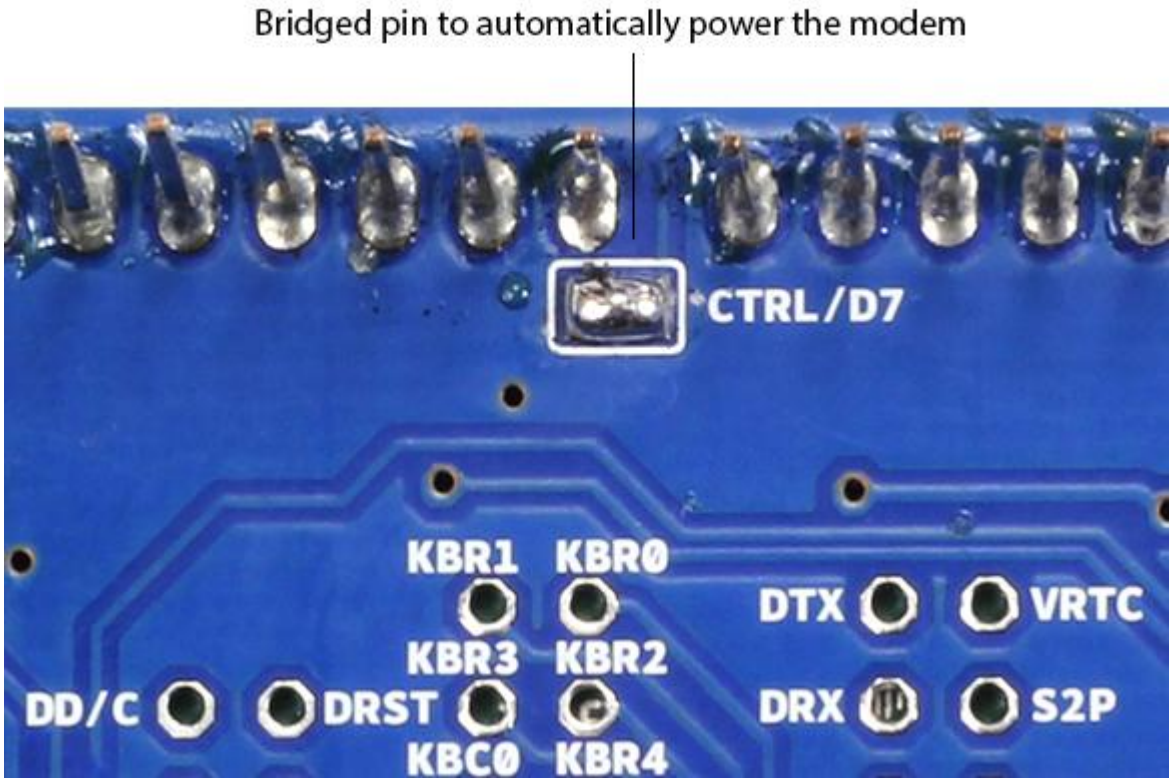
3.9.3 Earphone interface configuration





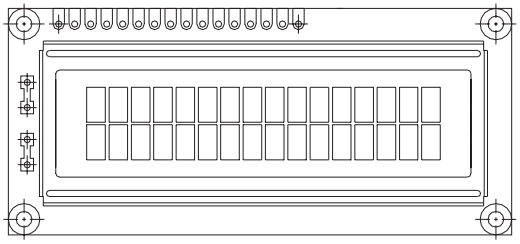


There are two small buttons on the shield. The button labelled "Reset" is tied to the Arduino reset pin. When pressed, it will restart the sketch. The button labelled "Power" is connected to the modem and will power the modem on and off. For early versions of the shield, it was necessary to press the *power* button to turn on the modem. Newer versions of the board will turn the modem on automatically.
If you have an early version of the shield, and it does not turn on automatically, you can solder a jumper to the CTRL/D7 pad on the reverse side of the board, and it will turn on when an attached Arduino receives power.



Several of the modem pins are exposed on the underside of the board. These provide access to the modem for features like speaker output and microphone input. See the datasheet for complete information.

16 x 2 Character LCD



FEATURES

- 5 x 8 dots with cursor
- Built-in controller (KS 0066 or Equivalent)
- + 5V power supply (Also available for + 3V)
- 1/16 duty cycle
- B/L to be driven by pin 1, pin 2 or pin 15, pin 16 or A.K (LED)
- N.V. optional for + 3V power supply

MECHANICAL DATA

ITEM	STANDARD VALUE	UNIT
Module Dimension	80.0 x 36.0	mm
Viewing Area	66.0 x 16.0	mm
Dot Size	0.56 x 0.66	mm
Character Size	2.96 x 5.56	mm

ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	STANDARD VALUE			UNIT
		MIN.	TYP.	MAX.	
Power Supply	VDD-VSS	- 0.3	–	7.0	V
Input Voltage	VI	- 0.3	–	VDD	V

NOTE: VSS = 0 Volt, VDD = 5.0 Volt

ELECTRICAL SPECIFICATIONS

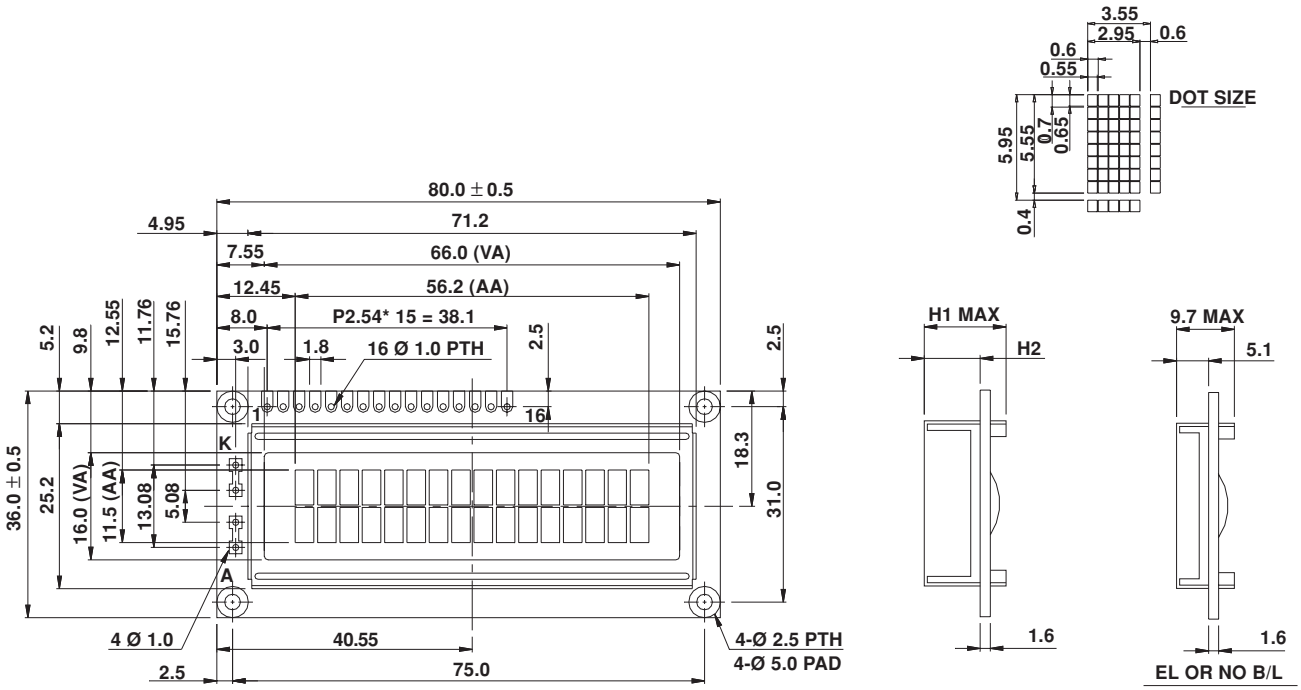
ITEM	SYMBOL	CONDITION		STANDARD VALUE			UNIT
				MIN.	TYP.	MAX.	
Input Voltage	VDD	VDD = + 5V		4.7	5.0	5.3	V
		VDD = + 3V		2.7	3.0	5.3	V
Supply Current	IDD	VDD = 5V		–	1.2	3.0	mA
Recommended LC Driving Voltage for Normal Temp. Version Module	VDD - V0	- 20 °C		–	–	–	V
		0°C		4.2	4.8	5.1	
		25°C		3.8	4.2	4.6	
		50°C		3.6	4.0	4.4	
		70°C		–	–	–	
LED Forward Voltage	VF	25°C		–	4.2	4.6	V
LED Forward Current	IF	25°C	Array	–	130	260	mA
			Edge	–	20	40	
EL Power Supply Current	IEL	Vel = 110VAC:400Hz		–	–	5.0	mA

DISPLAY CHARACTER ADDRESS CODE:

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01														0F
DD RAM Address	40	41														4F

PIN NUMBER	SYMBOL	FUNCTION
1	Vss	GND
2	Vdd	+ 3V or + 5V
3	Vo	Contrast Adjustment
4	RS	H/L Register Select Signal
5	R/$\overline{W}$	H/L Read/Write Signal
6	E	H →L Enable Signal
7	DB0	H/L Data Bus Line
8	DB1	H/L Data Bus Line
9	DB2	H/L Data Bus Line
10	DB3	H/L Data Bus Line
11	DB4	H/L Data Bus Line
12	DB5	H/L Data Bus Line
13	DB6	H/L Data Bus Line
14	DB7	H/L Data Bus Line
15	A/Vee	+ 4.2V for LED/Negative Voltage Output
16	K	Power Supply for B/L (OV)

DIMENSIONS in millimeters



LED - H/L B/L		
	HIGH	LOW
H1	13.2	12.1
H2	8.6	7.5

MFRC522

Standard performance MIFARE and NTAG frontend

Rev. 3.9 — 27 April 2016
112139

Product data sheet
COMPANY PUBLIC

1. Introduction

This document describes the functionality and electrical specifications of the contactless reader/writer MFRC522.

Remark: The MFRC522 supports all variants of the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus RF identification protocols. To aid readability throughout this data sheet, the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus products and protocols have the generic name MIFARE.

1.1 Differences between version 1.0 and 2.0

The MFRC522 is available in two versions:

- MFRC52201HN1, hereafter referred to version 1.0 and
- MFRC52202HN1, hereafter referred to version 2.0.

The MFRC522 version 2.0 is fully compatible to version 1.0 and offers in addition the following features and improvements:

- Increased stability of the reader IC in rough conditions
- An additional timer prescaler, see Section 8.5.
- A corrected CRC handling when RX Multiple is set to 1

This data sheet version covers both versions of the MFRC522 and describes the differences between the versions if applicable.

2. General description

The MFRC522 is a highly integrated reader/writer IC for contactless communication at 13.56 MHz. The MFRC522 reader supports ISO/IEC 14443 A/MIFARE and NTAG.

The MFRC522's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

The MFRC522 supports MF1xxS20, MF1xxS70 and MF1xxS50 products. The MFRC522 supports contactless communication and uses MIFARE higher transfer speeds up to 848 kBd in both directions.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependant on pin voltage supply)
- I^2C-bus interface

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE and NTAG
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports MF1xxS20, MF1xxS70 and MF1xxS50 encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication up to 848 kBd
- Supports MFIN/MFOUT
- Additional internal power supply to the smart card IC connected via MFIN/MFOUT
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage			2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage		[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	µA
		soft power-down; RF level detector on	[4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; $V_{DDD} = 3$ V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[5]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T_{amb}	ambient temperature	HVQFN32		−25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[6] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[7] During typical circuit operation, the overall current is below 100 mA.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
MFRC52201HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52201HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52202HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52202HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

[1] Delivered in one tray.

[2] Delivered in five trays.

6. Block diagram

The analog interface handles the modulation and demodulation of the analog signals.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

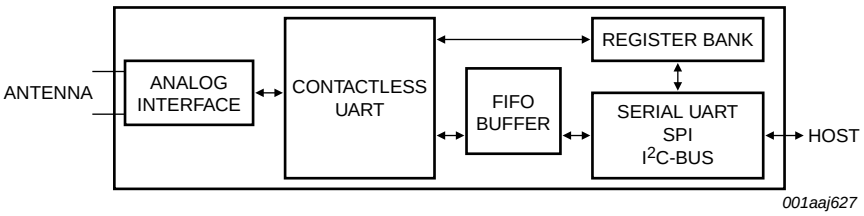


Fig 1. Simplified block diagram of the MFRC522

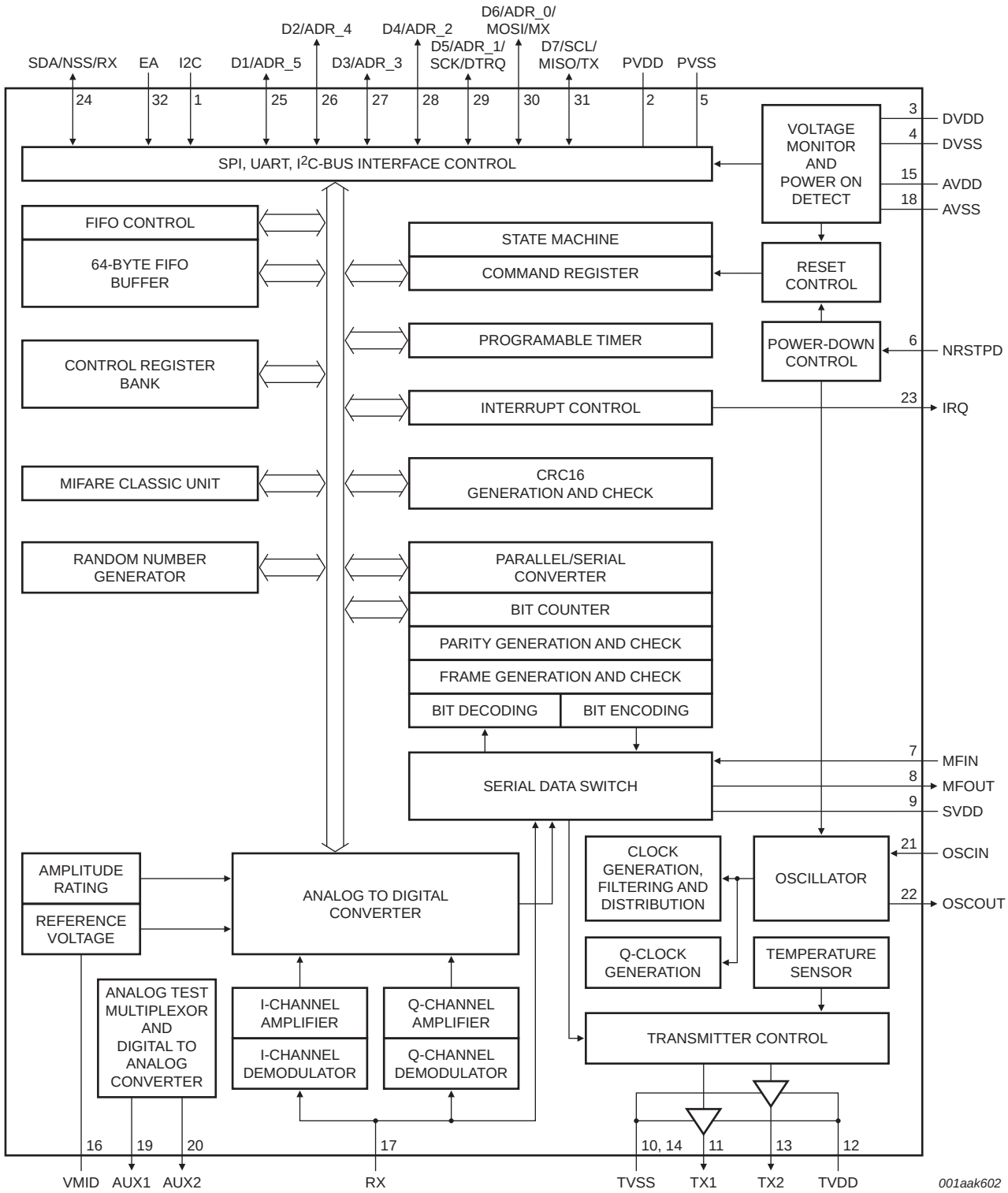
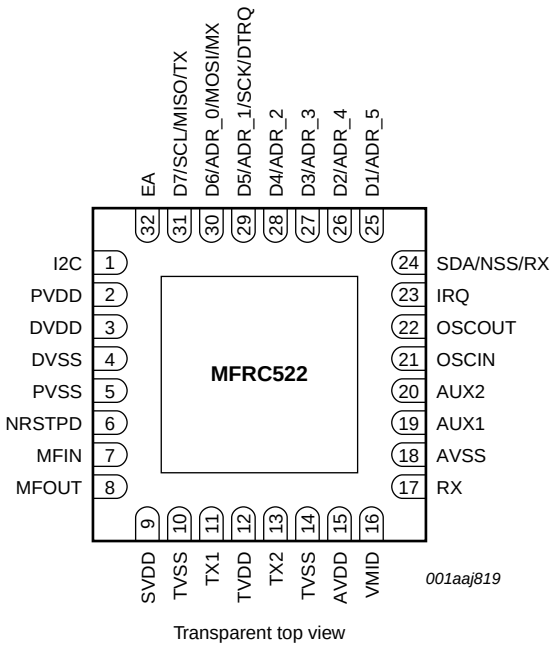


Fig 2. Detailed block diagram of the MFRC522

7. Pinning information



Transparent top view

Fig 3. Pinning configuration HVQFN32 (SOT617-1)

7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type[1]	Description
1	I2C	I	I^2C-bus enable input[2]
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G	digital ground[3]
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world reset: enabled by a positive edge
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	P	MFIN and MFOUT pin power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply

Table 3. Pin description *...continued*

Pin	Symbol	Type[1]	Description
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock (f_{clk} = 27.12 MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	SDA	I/O	I^2C-bus serial data line input/output[2]
	NSS	I	SPI signal input[2]
	RX	I	UART address input[2]
25	D1	I/O	test port[2]
	ADR_5	I/O	I^2C-bus address 5 input[2]
26	D2	I/O	test port
	ADR_4	I	I^2C-bus address 4 input[2]
27	D3	I/O	test port
	ADR_3	I	I^2C-bus address 3 input[2]
28	D4	I/O	test port
	ADR_2	I	I^2C-bus address 2 input[2]
29	D5	I/O	test port
	ADR_1	I	I^2C-bus address 1 input[2]
	SCK	I	SPI serial clock input[2]
	DTRQ	O	UART request to send output to microcontroller[2]
30	D6	I/O	test port
	ADR_0	I	I^2C-bus address 0 input[2]
	MOSI	I/O	SPI master out, slave in[2]
	MX	O	UART output to microcontroller[2]
31	D7	I/O	test port
	SCL	I/O	I^2C-bus clock input/output[2]
	MISO	I/O	SPI master in, slave out[2]
	TX	O	UART data output to microcontroller[2]
32	EA	I	external address input for coding I^2C-bus address[2]

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] The pin functionality of these pins is explained in Section 8.1 “Digital interfaces”.

[3] Connection of heatsink pad on package bottom side is not necessary. Optional connection to pin DVSS is possible.

8. Functional description

The MFRC522 transmission module supports the Read/Write mode for ISO/IEC 14443 A/MIFARE using various transfer speeds and modulation protocols.

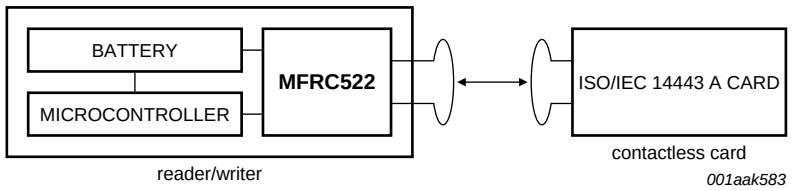
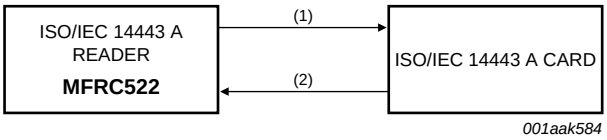


Fig 4. MFRC522 Read/Write mode

The physical level communication is shown in Figure 5.



(1) Reader to card 100 % ASK, Miller encoded, transfer speed 106 kBd to 848 kBd.

(2) Card to reader subcarrier load modulation, Manchester encoded or BPSK, transfer speed 106 kBd to 848 kBd.

Fig 5. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (send data from the MFRC522 to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 μs)	64 (13.56 μs)	32 (13.56 μs)	16 (13.56 μs)
Card to reader (MFRC522 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The MFRC522's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. Figure 6 shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.

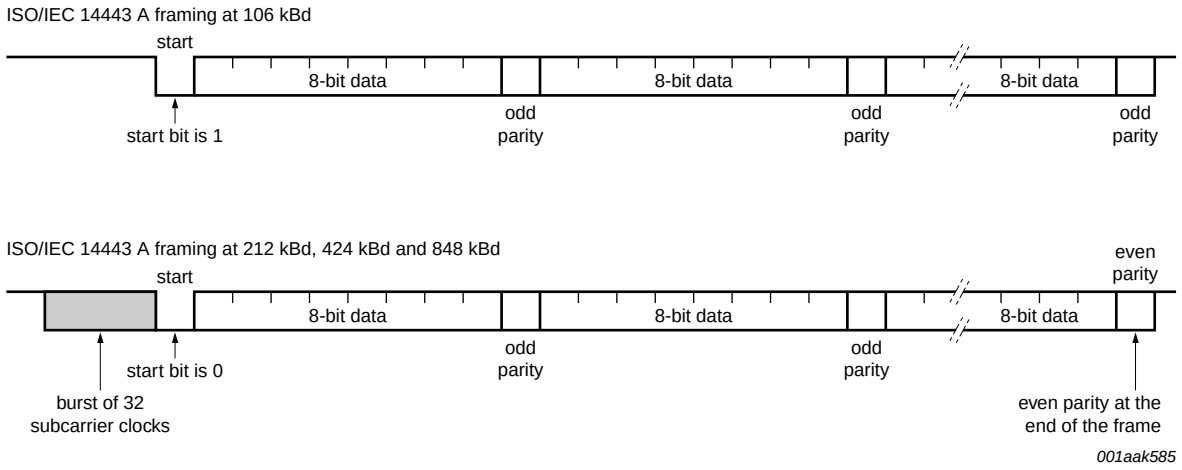


Fig 6. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the MfRxReg register's ParityDisable bit.

8.1 Digital interfaces

8.1.1 Automatic microcontroller interface detection

The MFRC522 supports direct interfacing of hosts using SPI, I^2C-bus or serial UART interfaces. The MFRC522 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The MFRC522 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 5 shows the different connection configurations.

Table 5. Connection protocol for detecting different interface types

Pin	Interface type		
	UART (input)	**SPI (output)**	**I^2C-bus (I/O)**
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

8.1.2 Serial Peripheral Interface

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the MFRC522 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MFRC522 and a microcontroller. The implemented interface is in accordance with the SPI standard.

The timing specification is given in Section 14.1 on page 78.

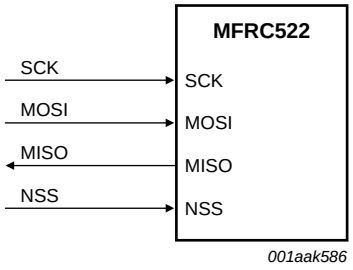


Fig 7. SPI connection to host

The MFRC522 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MFRC522 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the MFRC522 on the falling clock edge and is stable during the rising clock edge.

8.1.2.1 SPI read data

Reading data using SPI requires the byte order shown in Table 6 to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

Table 6. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X[1]	data 0	data 1	...	data n − 1	data n

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.2 SPI write data

To write data to the MFRC522 using SPI requires the byte order shown in Table 7. It is possible to write up to n data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 7. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n – 1	data n
MISO	X[1]	X[1]	X[1]	...	X[1]	X[1]

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.3 SPI address byte

The address byte must meet the following format.

The MSB of the first byte defines the mode used. To read data from the MFRC522 the MSB is set to logic 1. To write data to the MFRC522 the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

Table 8. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	address						0

8.1.3 UART interface

8.1.3.1 Connection to a host

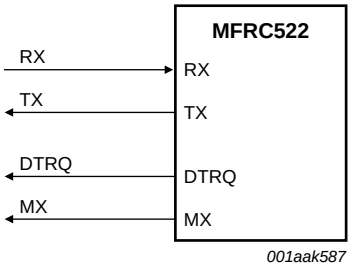


Fig 8. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.1.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

The BR_T0[2:0] and BR_T1[4:0] settings are described in Table 9. Examples of different transfer speeds and the relevant register settings are given in Table 10.

Table 9. BR_T0 and BR_T1 settings

BR_Tn	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 10. Selectable UART transfer speeds

Transfer speed (kBd)	SerialSpeedReg value		Transfer speed accuracy (%)[1]
	Decimal	Hexadecimal	
7.2	250	FAh	–0.25
9.6	235	EBh	0.32
14.4	218	DAh	–0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	–0.25
115.2	122	7Ah	–0.25
128	116	74h	–0.06
230.4	90	5Ah	–0.25
460.8	58	3Ah	–0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds shown in Table 10 are calculated according to the following equations:

If BR_T0[2:0] = 0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR\_T0 + 1)} \quad (1)$$

If BR_T0[2:0] > 0:

$$transfer\ speed = \left(\frac{27.12 \times 10^6}{(BR\_T1 + 33)} \right) \Big/ 2^{(BR\_T0 - 1)} \quad (2)$$

Remark: Transfer speeds above 1228.8 kBd are not supported.

8.1.3.3 UART framing

Table 11. UART framing

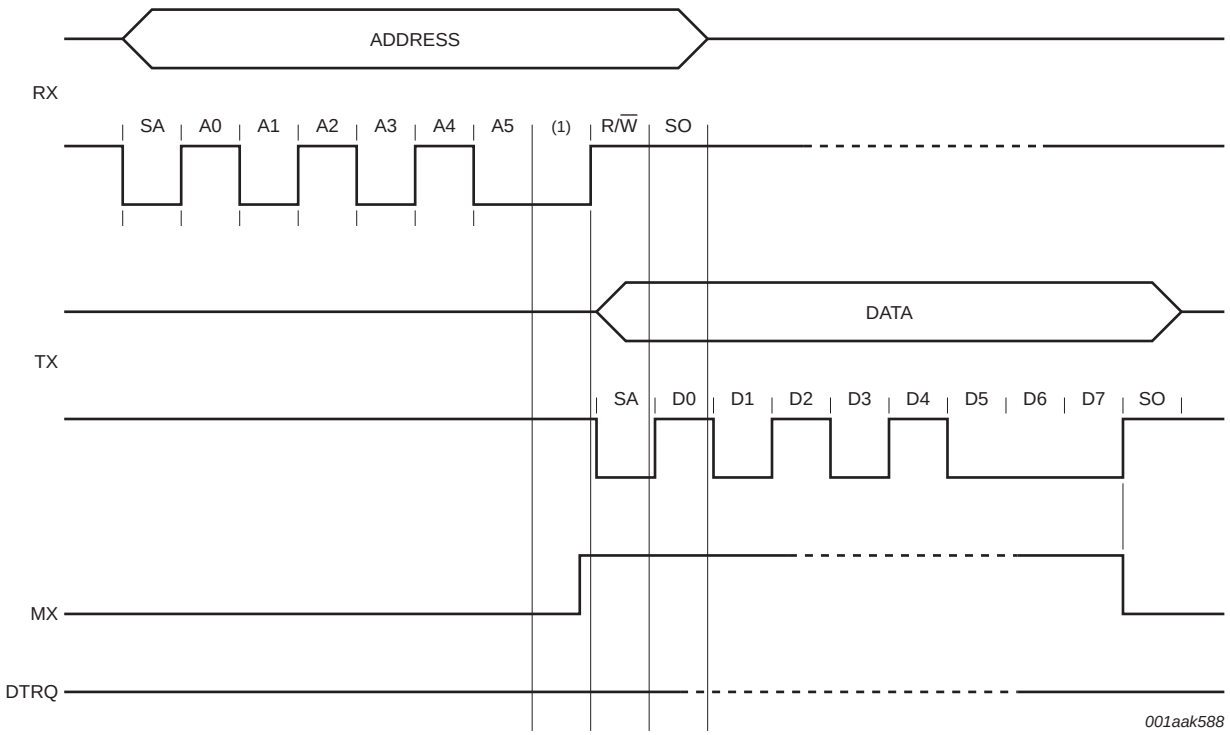
Bit	Length	Value
Start	1-bit	0
Data	8 bits	data
Stop	1-bit	1

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

Read data: To read data using the UART interface, the flow shown in Table 12 must be used. The first byte sent defines both the mode and the address.

Table 12. Read data byte order

Pin	Byte 0	Byte 1
RX (pin 24)	address	-
TX (pin 31)	-	data 0



(1) Reserved.

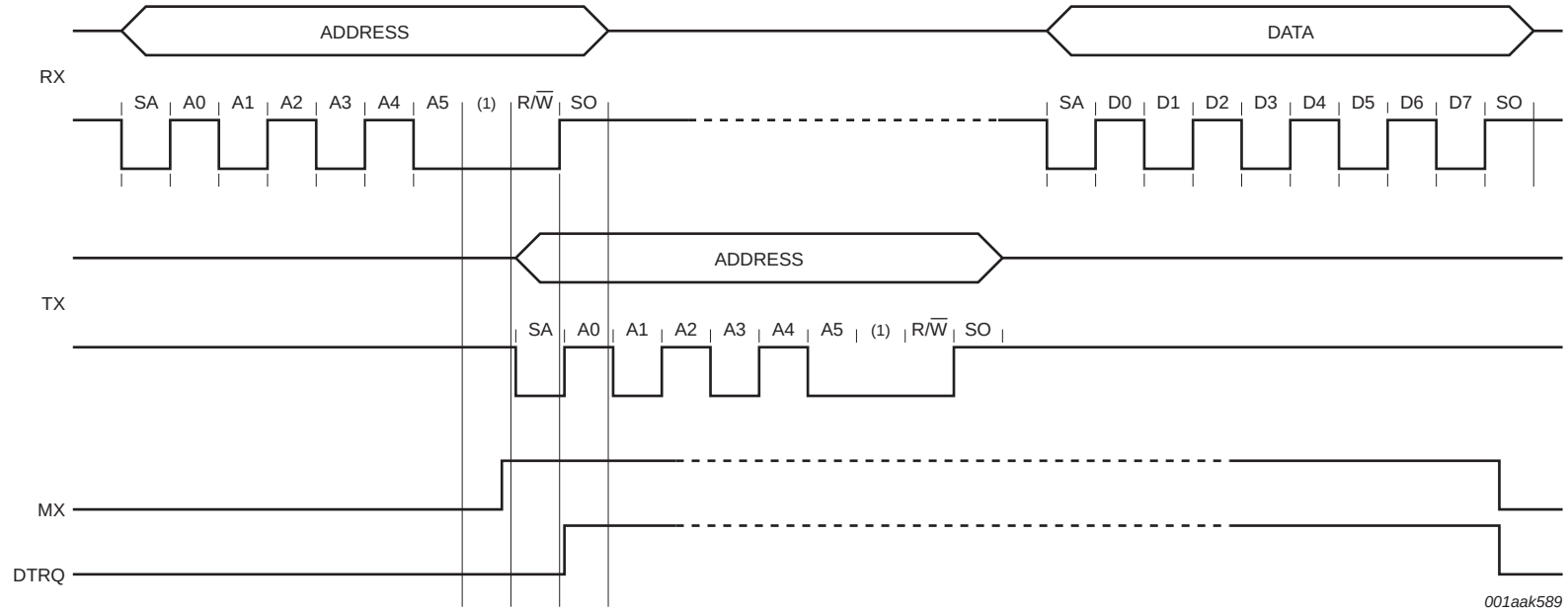
Fig 9. UART read data timing diagram

Write data: To write data to the MFRC522 using the UART interface, the structure shown in Table 13 must be used.

The first byte sent defines both the mode and the address.

Table 13. Write data byte order

Pin	Byte 0	Byte 1
RX (pin 24)	address 0	data 0
TX (pin 31)	-	address 0



(1) Reserved.

Fig 10. UART write data timing diagram

Remark: The data byte can be sent directly after the address byte on pin RX.

Address byte: The address byte has to meet the following format:

The MSB of the first byte sets the mode used. To read data from the MFRC522, the MSB is set to logic 1. To write data to the MFRC522 the MSB is set to logic 0. Bit 6 is reserved for future use, and bits 5 to 0 define the address; see Table 14.

Table 14. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	reserved	address					

8.1.4 I²C-bus interface

An I²C-bus (Inter-IC) interface is supported to enable a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented according to NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in Slave mode. Therefore the MFRC522 does not implement clock generation or access arbitration.

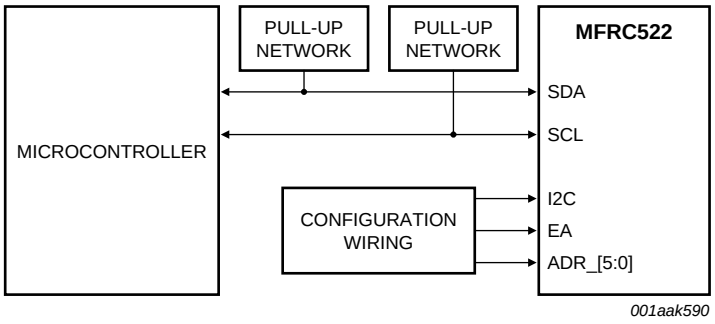


Fig 11. I²C-bus interface

The MFRC522 can act either as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MFRC522 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

See Table 155 on page 79 for timing requirements.

8.1.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

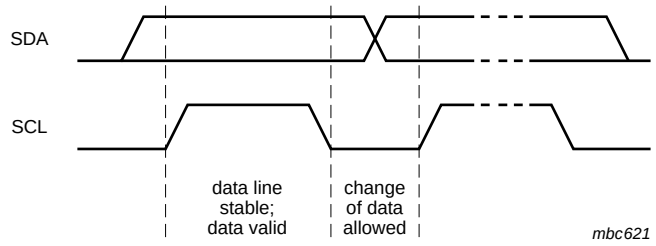


Fig 12. Bit transfer on the I²C-bus

8.1.4.2 START and STOP conditions

To manage the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

- A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.
- A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I²C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

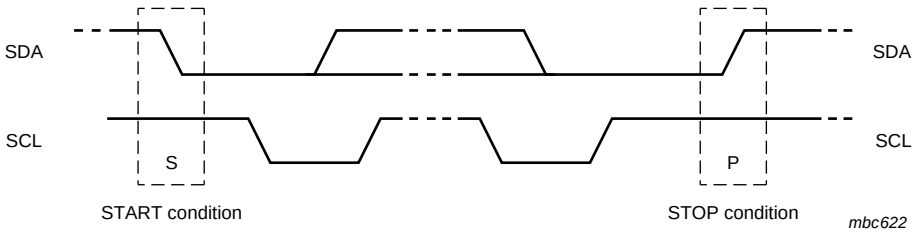


Fig 13. START and STOP conditions

8.1.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see Figure 16. The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

8.1.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

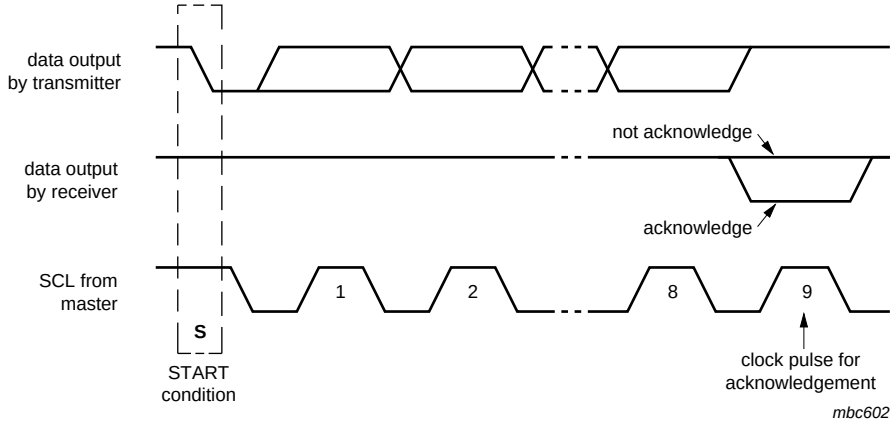


Fig 14. Acknowledge on the I²C-bus

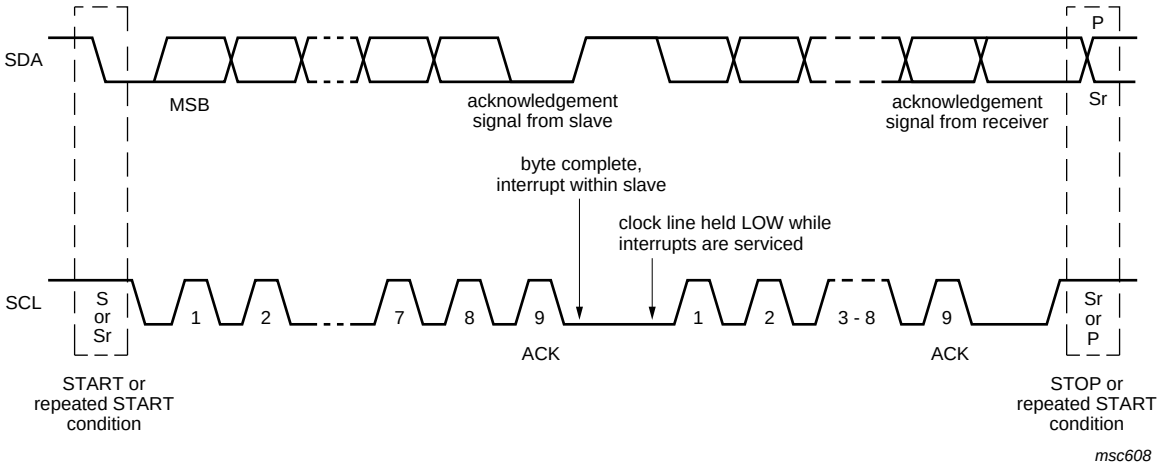


Fig 15. Data transfer on the I²C-bus

8.1.4.5 7-Bit addressing

During the I²C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the *I²C-bus specification* for a complete list of reserved addresses.

The I²C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I²C-bus address according to pin EA.

If pin EA is set LOW, the upper 4 bits of the device bus address are reserved by NXP Semiconductors and set to 0101b for all MFRC522 devices. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with other I²C-bus devices.

If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins according to Table 5 on page 9. ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C-bus address pins can be used for test signal outputs.

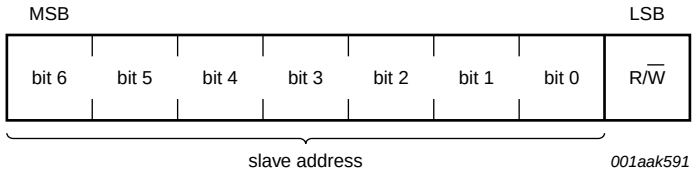


Fig 16. First byte following the START procedure

8.1.4.6 Register write access

To write data from the host controller using the I²C-bus to a specific register in the MFRC522 the following frame format must be used.

- The first byte of a frame indicates the device address according to the I²C-bus rules.
- The second byte indicates the register address followed by up to n-data bytes.

In one frame all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/$\overline{W}$) bit is set to logic 0.

8.1.4.7 Register read access

To read out data from a specific register address in the MFRC522, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I²C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of the MFRC522. In response, the MFRC522 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

The Read/Write (R/W) bit is set to logic 1.

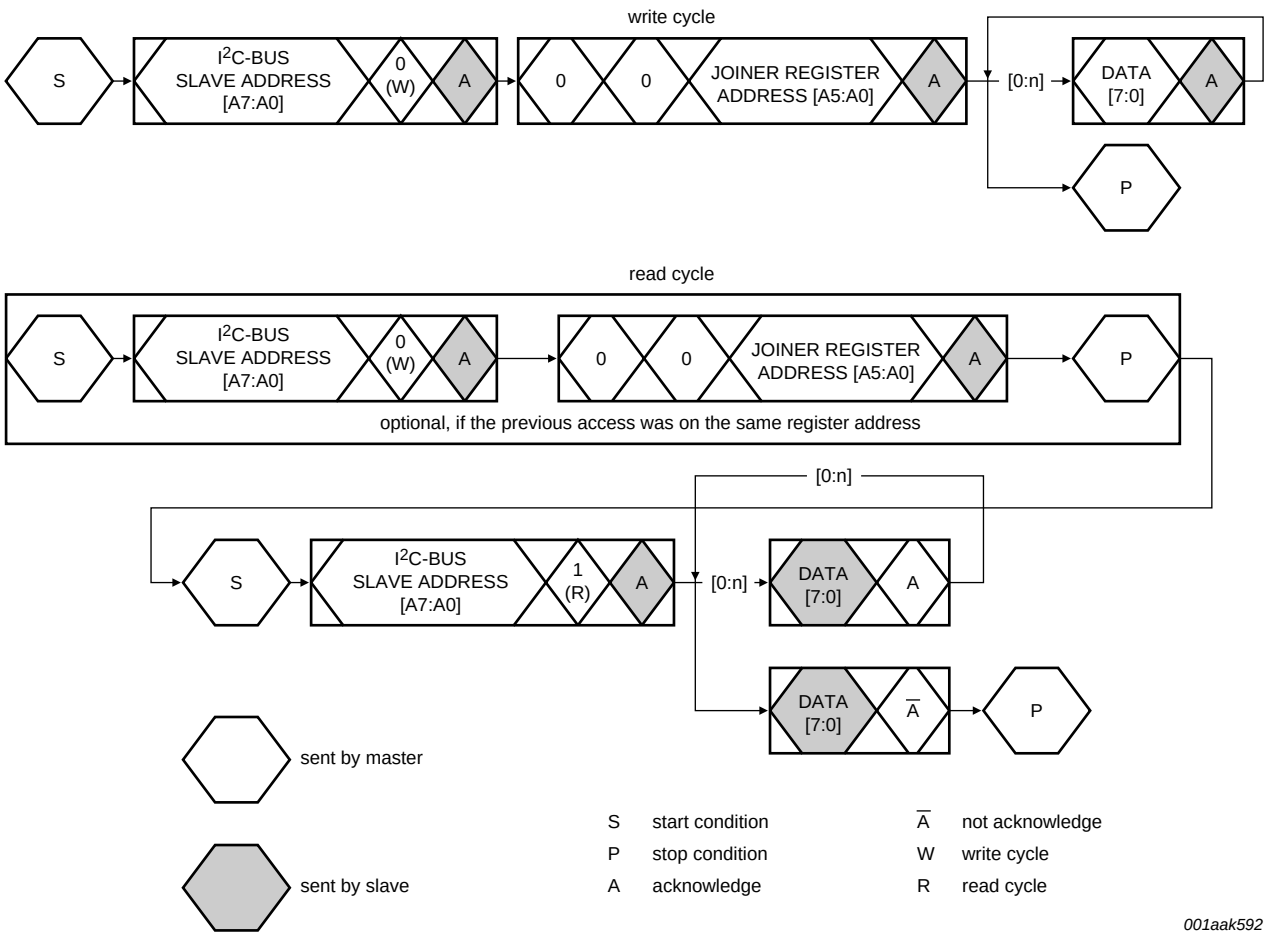


Fig 17. Register read and write access

8.1.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard mode (F/S mode) for bidirectional communication in a mixed-speed bus system.

8.1.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I^2C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

8.1.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I^2C-bus specification. HS mode can only start after all of the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001XXXb)
3. Not-acknowledge bit ($\overline{A}$)

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected MFRC522.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

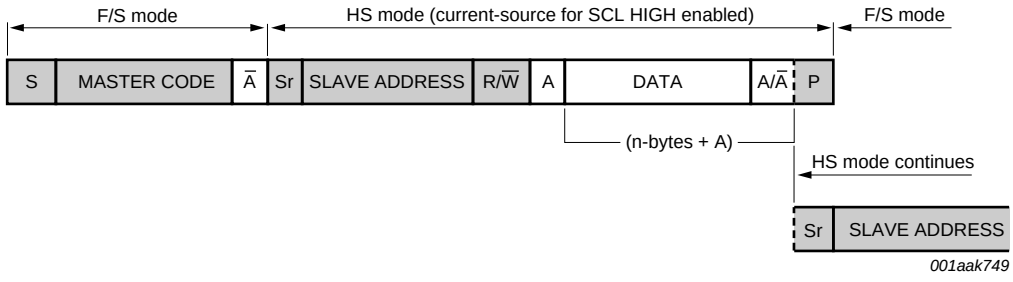


Fig 18. I^2C-bus HS mode protocol switch

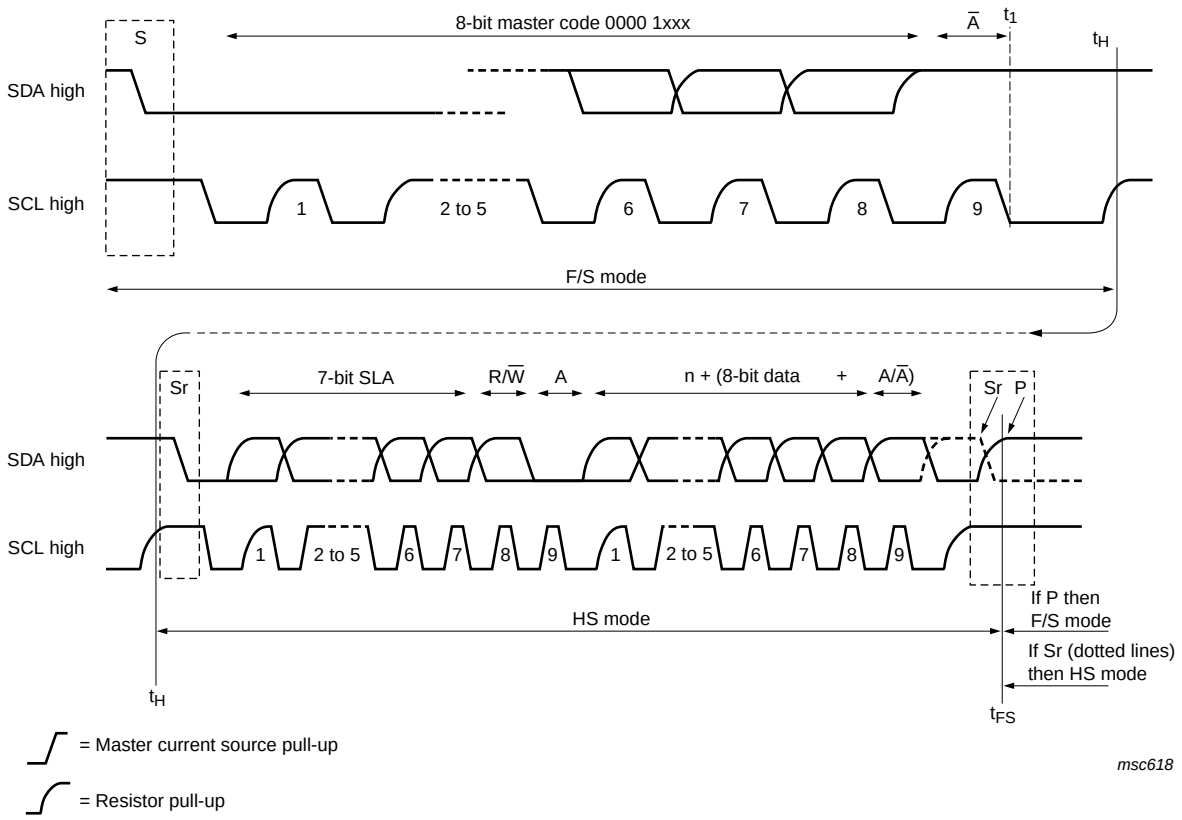


Fig 19. I²C-bus HS mode protocol frame

8.1.4.11 Switching between F/S mode and HS mode

After reset and initialization, the MFRC522 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected MFRC522 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I^2C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register’s I^2CForceHS bit to logic 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I^2C-bus lines must be avoided because of the reduced spike suppression.

8.1.4.12 MFRC522 at lower speed modes

MFRC522 is fully downward-compatible and can be connected to an F/S mode I^2C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

8.2 Analog interface and contactless UART

8.2.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.

Remark: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

8.2.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering; see Section 15 on page 81. The signal on pins TX1 and TX2 can be configured using the TxControlReg register; see Section 9.3.2.5 on page 50.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Table 15. Register and bit settings controlling the signal on pin TX1

Bit Tx1RFEn	Bit Force 100ASK	Bit InvTx1RFOn	Bit InvTx1RFOff	Envelope	Pin TX1	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	X[1]	0	RF	pMod	nMod	100 % ASK: pin TX1 pulled to logic 0, independent of the InvTx1RFOff bit
				1	RF	pCW	nCW	
	0	1	X[1]	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	X[1]	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

[1] X = Do not care.

Table 16. Register and bit settings controlling the signal on pin TX2

Bit Tx1RFEn	Bit Force 100ASK	Bit Tx2CW	Bit InvTx2RFOn	Bit InvTx2RFOff	Envelope	Pin TX2	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	0	X[1]	0	RF	pMod	nMod	-
					1	RF	pCW	nCW	
			1	X[1]	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	conductance always CW for the Tx2CW bit
			1	X[1]	X[1]	RF_n	pCW	nCW	
	1	0	0	X[1]	0	0	pMod	nMod	100 % ASK: pin TX2 pulled to logic 0 (independent of the InvTx2RFOn/InvTx2RFOff bits)
					1	RF	pCW	nCW	
			1	X[1]	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	
			1	X[1]	X[1]	RF_n	pCW	nCW	

[1] X = Do not care.

The following abbreviations have been used in Table 15 and Table 16:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2
- RF_n: inverted 13.56 MHz clock
- GSPMos: conductance, configuration of the PMOS array
- GSNMos: conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register
- nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits
- nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits
- X = do not care.

Remark: If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers.

8.2.3 Serial data switch

Two main blocks are implemented in the MFRC522. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins MFIN and MFOUT.

This topology allows the analog block of the MFRC522 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 20 shows the serial data switch for p-driver TX1 and TX2.

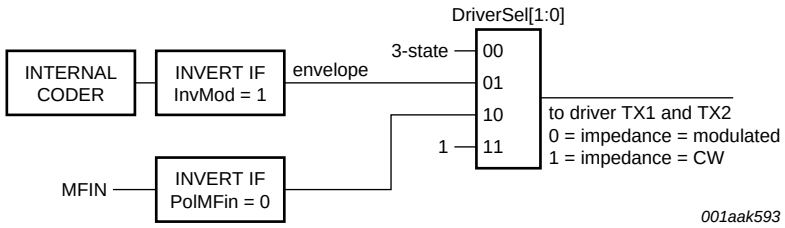


Fig 20. Serial data switch for p-driver TX1 and TX2

8.2.4 MFIN and MFOUT interface support

The MFRC522 is divided into a digital circuit block and an analog circuit block. The digital block contains state machines, encoder and decoder logic and so on. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured so that the interfacing signals can be routed to pins MFIN and MFOUT; see Figure 21 on page 28. This configuration is implemented using TxSelReg register's MFOutSel[3:0] and DriverSel[1:0] bits and RxSelReg register's UARTSel[1:0] bits.

This topology allows some parts of the analog block to be connected to the digital block of another device.

Switch MFOutSel in the TxSelReg register can be used to measure MIFARE and ISO/IEC14443 A related signals. This is especially important during the design-in phase or for test purposes as it enables checking of the transmitted and received data.

The most important use of pins MFIN and MFOUT is found in the active antenna concept. An external active antenna circuit can be connected to the MFRC522's digital block. Switch MFOutSel must be configured so that the internal Miller encoded signal is sent to pin MFOUT (MFOutSel = 100b). UARTSel[1:0] must be configured to receive a Manchester signal with subcarrier from pin MFIN (UARTSel[1:0] = 01).

It is possible to connect a passive antenna to pins TX1, TX2 and RX (using the appropriate filter and matching circuit) and an active antenna to pins MFOUT and MFIN at the same time. In this configuration, two RF circuits can be driven (one after another) by a single host processor.

Remark: Pins MFIN and MFOUT have a dedicated supply on pin SVDD with the ground on pin PVSS. If pin MFIN is not used it must be connected to either pin SVDD or pin PVSS. If pin SVDD is not used it must be connected to either pin DVDD, pin PVDD or any other voltage supply pin.

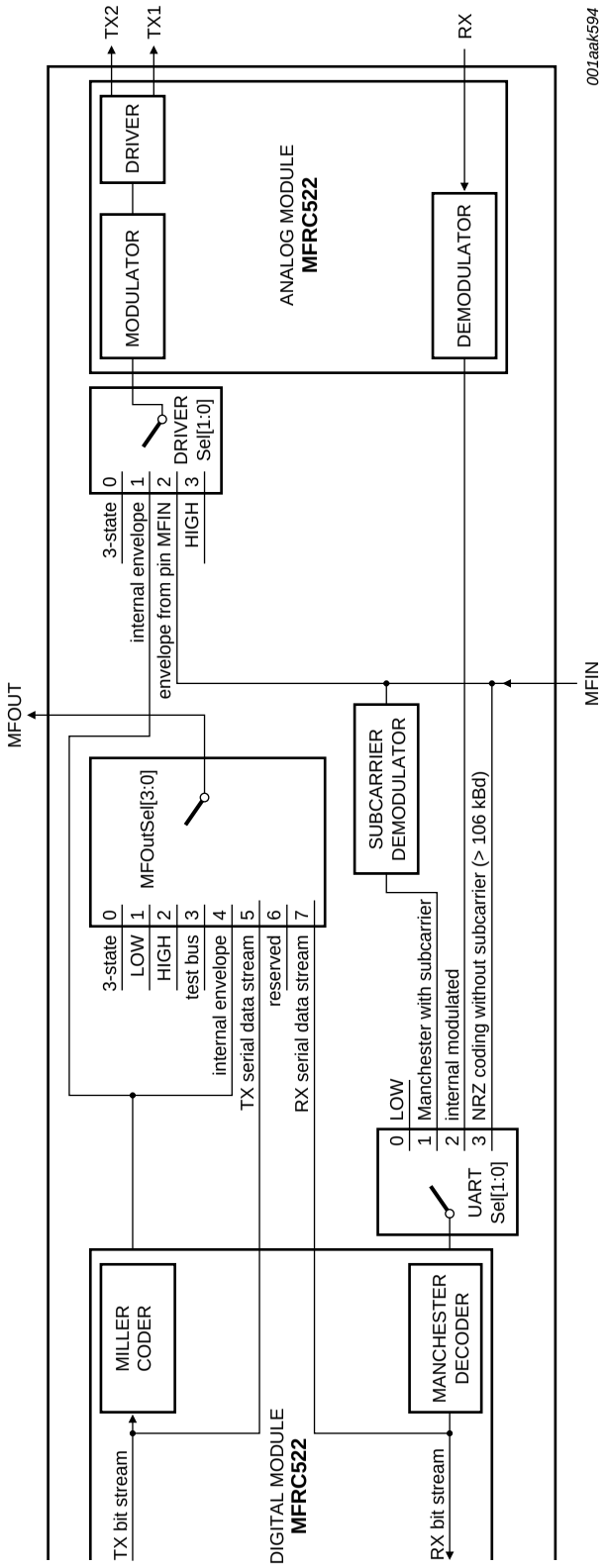


Fig 21. Overview of MFIN and MFOUT signal routing

8.2.5 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSBFirst bit indicates that data will be loaded with the MSB first.

Table 17. CRC coprocessor parameters

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

8.3 FIFO buffer

An 8 × 64 bit FIFO buffer is used in the MFRC522. It buffers the input and output data stream between the host and the MFRC522's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

8.3.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the MFRC522 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

8.3.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bit to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorReg register's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

8.3.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0]
- FIFO buffer almost full warning: Status1Reg register's HiAlert bit

- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The MFRC522 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to logic 1.
- ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to logic 1.

If the maximum number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. It is generated according to Equation 3:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel \quad (3)$$

If the number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1. It is generated according to Equation 4:

$$LoAlert = FIFOLength \leq WaterLevel \quad (4)$$

8.4 Interrupt request system

The MFRC522 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

8.4.1 Interrupt sources overview

Table 18 shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle (see Table 149 on page 70).

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register's HiAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register's LoAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

Table 18. Interrupt sources

Interrupt flag	Interrupt source	Trigger action
IRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIrqReg register	command execution finishes
HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

8.5 Timer unit

The MFRC522A has a timer unit which the external host can use to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Timeout counter
- Watchdog counter
- Stop watch
- Programmable one shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events explained in the paragraphs below. The timer does not influence any internal events, for example, a time-out during data reception does not automatically influence the reception process. Furthermore, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 13.56 MHz derived from the 27.12 MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

The prescaler (TPrescaler) is a 12-bit counter. The reload values (TReloadVal_Hi[7:0] and TReloadVal_Lo[7:0]) for TPrescaler can be set between 0 and 4095 in the TModeReg register's TPrescaler_Hi[3:0] bits and TPrescalerReg register's TPrescaler_Lo[7:0] bits.

The reload value for the counter is defined by 16 bits between 0 and 65535 in the TReloadReg register.

The current value of the timer is indicated in the TCounterValReg register.

When the counter reaches 0, an interrupt is automatically generated, indicated by the ComIrqReg register's TimerIRq bit setting. If enabled, this event can be indicated on pin IRQ. The TimerIRq bit can be set and reset by the host. Depending on the configuration, the timer will stop at 0 or restart with the value set in the TReloadReg register.

The timer status is indicated by the Status1Reg register's TRunning bit.

The timer can be started manually using the ControlReg register's TStartNow bit and stopped using the ControlReg register's TStopNow bit.

The timer can also be activated automatically to meet any dedicated protocol requirements by setting the TModeReg register's TAuto bit to logic 1.

The delay time of a timer stage is set by the reload value + 1. The total delay time (t_{d1}) is calculated using Equation 5:

$$t_{d1} = \frac{(TPrescaler \times 2 + 1) \times (TReloadVal + 1)}{13.56\ MHz} \quad (5)$$

An example of calculating total delay time (t_d) is shown in Equation 6, where the TPrescaler value = 4095 and TReloadVal = 65535:

$$39.59\ s = \frac{(4095 \times 2 + 1) \times (65535 + 1)}{13.56\ MHz} \quad (6)$$

Example: To give a delay time of 25 μs requires 339 clock cycles to be counted and a TPrescaler value of 169. This configures the timer to count up to 65535 time-slots for every 25 μs period.

The MFRC522 version 2.0 offers in addition a second prescaler timer. Due to the fact that the prescaler counts down to 0 the prescaler period always count an odd number of clocks (1, 3, 5, ..). This may lead to inaccuracy. The second available prescaler timer implements the possibility to change the prescaler reload value to odd numbers, which results in an even prescaler period. This new prescaler can be enabled only in version 2.0 using the register bit DemodeReg, see Table 72. Within this option, the total delay time (t_{d2}) is calculated using Equation 5:

$$t_{d2} = \frac{(TPrescaler \times 2 + 2) \times (TReloadVal + 1)}{13.56\ MHz} \quad (7)$$

8.6 Power reduction modes

8.6.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

8.6.2 Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the MFRC522 when Soft power-down mode is exited.

Remark: If the internal oscillator is used, you must take into account that it is supplied by pin AVDD and it will take a certain time (t_{osc}) until the oscillator is stable and the clock cycles can be detected by the internal logic. It is recommended for the serial UART, to first send the value 55h to the MFRC522. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the MFRC522 answers to the last read command with the register content of address 0. This indicates that the MFRC522 is ready.

8.6.3 Transmitter power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

8.7 Oscillator circuit

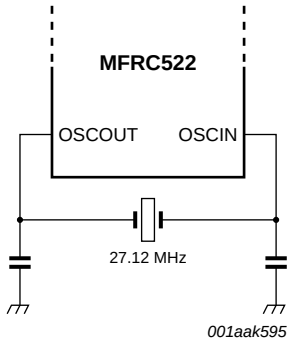


Fig 22. Quartz crystal connection

The clock applied to the MFRC522 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

8.8 Reset and oscillator start-up time

8.8.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

8.8.2 Oscillator start-up time

If the MFRC522 has been set to a Power-down mode or is powered by a V_{DDX} supply, the start-up time for the MFRC522 depends on the oscillator used and is shown in Figure 23.

The time ($t_{startup}$) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time (t_d) is the internal delay time of the MFRC522 when the clock signal is stable before the MFRC522 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27\ \mu s} = 37.74\ \mu s \tag{8}$$

The time (t_{osc}) is the sum of t_d and $t_{startup}$.

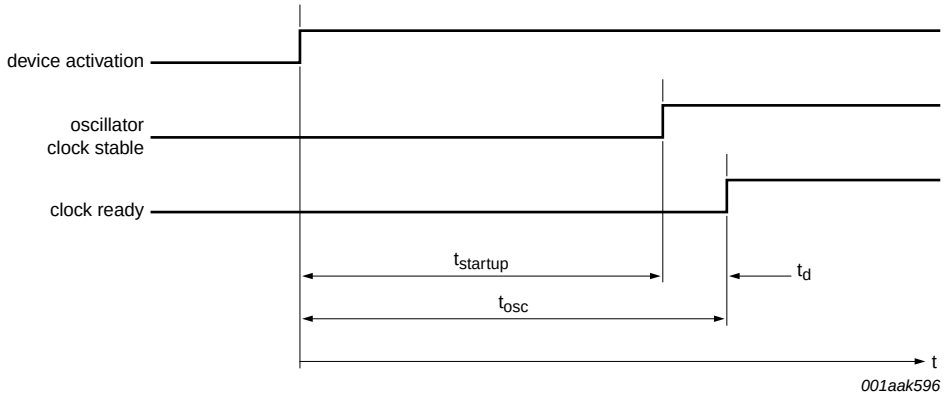


Fig 23. Oscillator start-up time

9. MFRC522 registers

9.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle, bits with same behavior are grouped in common registers. The access conditions are described in Table 19.

Table 19. Behavior of register bits and their designation

Abbreviation	Behavior	Description
R/W	read and write	These bits can be written and read by the microcontroller. Since they are used only for control purposes, their content is not influenced by internal state machines, for example the ComIEnReg register can be written and read by the microcontroller. It will also be read by internal state machines but never changed by them.
D	dynamic	These bits can be written and read by the microcontroller. Nevertheless, they can also be written automatically by internal state machines, for example the CommandReg register changes its value automatically after the execution of the command.
R	read only	These register bits hold values which are determined by internal states only, for example the CRCReady bit cannot be written externally but shows internal states.
W	write only	Reading these register bits always returns zero.
reserved	-	These registers are reserved for future use and must not be changed. In case of a write access, it is recommended to always write the value “0”.
RFT	-	These register bits are reserved for future use or are for production tests and must not be changed.

9.2 Register overview

Table 20. MFRC522 register overview

Address (hex)	Register name	Function	Refer to
Page 0: Command and status			
00h	Reserved	reserved for future use	Table 21 on page 38
01h	CommandReg	starts and stops command execution	Table 23 on page 38
02h	ComlEnReg	enable and disable interrupt request control bits	Table 25 on page 38
03h	DivlEnReg	enable and disable interrupt request control bits	Table 27 on page 39
04h	ComIrqReg	interrupt request bits	Table 29 on page 39
05h	DivIrqReg	interrupt request bits	Table 31 on page 40
06h	ErrorReg	error bits showing the error status of the last command executed	Table 33 on page 41
07h	Status1Reg	communication status bits	Table 35 on page 42
08h	Status2Reg	receiver and transmitter status bits	Table 37 on page 43
09h	FIFODataReg	input and output of 64 byte FIFO buffer	Table 39 on page 44
0Ah	FIFOLevelReg	number of bytes stored in the FIFO buffer	Table 41 on page 44
0Bh	WaterLevelReg	level for FIFO underflow and overflow warning	Table 43 on page 44
0Ch	ControlReg	miscellaneous control registers	Table 45 on page 45
0Dh	BitFramingReg	adjustments for bit-oriented frames	Table 47 on page 46
0Eh	CollReg	bit position of the first bit-collision detected on the RF interface	Table 49 on page 46
0Fh	Reserved	reserved for future use	Table 51 on page 47
Page 1: Command			
10h	Reserved	reserved for future use	Table 53 on page 47
11h	ModeReg	defines general modes for transmitting and receiving	Table 55 on page 48
12h	TxModeReg	defines transmission data rate and framing	Table 57 on page 48
13h	RxModeReg	defines reception data rate and framing	Table 59 on page 49
14h	TxControlReg	controls the logical behavior of the antenna driver pins TX1 and TX2	Table 61 on page 50
15h	TxASKReg	controls the setting of the transmission modulation	Table 63 on page 51
16h	TxSelReg	selects the internal sources for the antenna driver	Table 65 on page 51
17h	RxSelReg	selects internal receiver settings	Table 67 on page 52
18h	RxThresholdReg	selects thresholds for the bit decoder	Table 69 on page 53
19h	DemodReg	defines demodulator settings	Table 71 on page 53
1Ah	Reserved	reserved for future use	Table 73 on page 54
1Bh	Reserved	reserved for future use	Table 75 on page 54
1Ch	MfTxReg	controls some MIFARE communication transmit parameters	Table 77 on page 55
1Dh	MfRxReg	controls some MIFARE communication receive parameters	Table 79 on page 55
1Eh	Reserved	reserved for future use	Table 81 on page 55
1Fh	SerialSpeedReg	selects the speed of the serial UART interface	Table 83 on page 55
Page 2: Configuration			
20h	Reserved	reserved for future use	Table 85 on page 57

Table 20. MFRC522 register overview *…continued*

Address (hex)	Register name	Function	Refer to
21h	CRCResultReg	shows the MSB and LSB values of the CRC calculation	Table 87 on page 57
22h			Table 89 on page 57
23h	Reserved	reserved for future use	Table 91 on page 58
24h	ModWidthReg	controls the ModWidth setting	Table 93 on page 58
25h	Reserved	reserved for future use	Table 95 on page 58
26h	RFCfgReg	configures the receiver gain	Table 97 on page 59
27h	GsNReg	selects the conductance of the antenna driver pins TX1 and TX2 for modulation	Table 99 on page 59
28h	CWGsPReg	defines the conductance of the p-driver output during periods of no modulation	Table 101 on page 60
29h	ModGsPReg	defines the conductance of the p-driver output during periods of modulation	Table 103 on page 60
2Ah	TModeReg	defines settings for the internal timer	Table 105 on page 60
2Bh	TPrescalerReg		Table 107 on page 61
2Ch	TReloadReg	defines the 16-bit timer reload value	Table 109 on page 62
2Dh			Table 111 on page 62
2Eh	TCounterValReg	shows the 16-bit timer value	Table 113 on page 63
2Fh			Table 115 on page 63
Page 3: Test register			
30h	Reserved	reserved for future use	Table 117 on page 63
31h	TestSel1Reg	general test signal configuration	Table 119 on page 63
32h	TestSel2Reg	general test signal configuration and PRBS control	Table 121 on page 64
33h	TestPinEnReg	enables pin output driver on pins D1 to D7	Table 123 on page 64
34h	TestPinValueReg	defines the values for D1 to D7 when it is used as an I/O bus	Table 125 on page 65
35h	TestBusReg	shows the status of the internal test bus	Table 127 on page 65
36h	AutoTestReg	controls the digital self test	Table 129 on page 66
37h	VersionReg	shows the software version	Table 131 on page 66
38h	AnalogTestReg	controls the pins AUX1 and AUX2	Table 133 on page 67
39h	TestDAC1Reg	defines the test value for TestDAC1	Table 135 on page 68
3Ah	TestDAC2Reg	defines the test value for TestDAC2	Table 137 on page 68
3Bh	TestADCReg	shows the value of ADC I and Q channels	Table 139 on page 68
3Ch to 3Fh	Reserved	reserved for production tests	Table 141 to Table 147 on page 69

9.3 Register descriptions

9.3.1 Page 0: Command and status

9.3.1.1 Reserved register 00h

Functionality is reserved for future use.

Table 21. Reserved register (address 00h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 22. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	-	reserved

9.3.1.2 CommandReg register

Starts and stops command execution.

Table 23. CommandReg register (address 01h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		RcvOff	PowerDown	Command[3:0]			
Access:	-		R/W	D	D			

Table 24. CommandReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5	RcvOff	1	analog part of the receiver is switched off
4	PowerDown	1	Soft power-down mode entered
		0	MFRC522 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the MFRC522 is ready; see Section 8.6.2 on page 33 **Remark:** The PowerDown bit cannot be set when the SoftReset command is activated
3 to 0	Command[3:0]	-	activates a command based on the Command value; reading this register shows which command is executed; see Section 10.3 on page 70

9.3.1.3 ComIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 25. ComIEnReg register (address 02h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 26. ComIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRqInv	1	signal on pin IRQ is inverted with respect to the Status1Reg register's IRq bit
		0	signal on pin IRQ is equal to the IRq bit; in combination with the DivIEnReg register's IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state
6	TxIEn	-	allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ
5	RxIEn	-	allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ
4	IdleIEn	-	allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ
3	HiAlertIEn	-	allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ
2	LoAlertIEn	-	allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ
1	ErrIEn	-	allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ
0	TimerIEn	-	allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ

9.3.1.4 DivIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 27. DivIEnReg register (address 03h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRQPushPull	reserved		MfinActIEn	reserved	CRCIEn	reserved	
Access	R/W	-		R/W	-	R/W	-	

Table 28. DivIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRQPushPull	1	pin IRQ is a standard CMOS output pin
		0	pin IRQ is an open-drain output pin
6 to 5	reserved	-	reserved for future use
4	MfinActIEn	-	allows the MFIN active interrupt request to be propagated to pin IRQ
3	reserved	-	reserved for future use
2	CRCIEn	-	allows the CRC interrupt request, indicated by the DivIrqReg register's CRCIRq bit, to be propagated to pin IRQ
1 to 0	reserved	-	reserved for future use

9.3.1.5 ComIrqReg register

Interrupt request bits.

Table 29. ComIrqReg register (address 04h); reset value: 14h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access	W	D	D	D	D	D	D	D

Table 30. ComIrqReg register bit descriptions

All bits in the ComIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set1	1	indicates that the marked bits in the ComIrqReg register are set
		0	indicates that the marked bits in the ComIrqReg register are cleared
6	TxIRq	1	set immediately after the last bit of the transmitted data was sent out
5	RxIRq	1	receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are available in the FIFO
4	IdleIRq	1	If a command terminates, for example, when the CommandReg changes its value from any command to the Idle command (see Table 149 on page 70) if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set The microcontroller starting the Idle command does not set the IdleIRq bit
3	HiAlertIRq	1	the Status1Reg register's HiAlert bit is set in opposition to the HiAlert bit, the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
2	LoAlertIRq	1	Status1Reg register's LoAlert bit is set in opposition to the LoAlert bit, the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
1	ErrIRq	1	any error bit in the ErrorReg register is set
0	TimerIRq	1	the timer decrements the timer value in register TCounterValReg to zero

9.3.1.6 DivIrqReg register

Interrupt request bits.

Table 31. DivIrqReg register (address 05h); reset value: x0h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set2	reserved		MfinActIRq	reserved	CRCIRq	reserved	
Access	W	-		D	-	D	-	

Table 32. DivIrqReg register bit descriptions

All bits in the DivIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set2	1	indicates that the marked bits in the DivIrqReg register are set
		0	indicates that the marked bits in the DivIrqReg register are cleared
6 to 5	reserved	-	reserved for future use
4	MfinActIRq	1	MFIN is active this interrupt is set when either a rising or falling signal edge is detected
3	reserved	-	reserved for future use
2	CRCIRq	1	the CalcCRC command is active and all data is processed
1 to 0	reserved	-	reserved for future use

9.3.1.7 ErrorReg register

Error bit register showing the error status of the last command executed.

Table 33. ErrorReg register (address 06h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	reserved	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access	R	R	-	R	R	R	R	R

Table 34. ErrorReg register bit descriptions

Bit	Symbol	Value	Description
7	WrErr	1	data is written into the FIFO buffer by the host during the MFAuthent command or if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface
6	TempErr[1]	1	internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off
5	reserved	-	reserved for future use
4	BufferOvfl	1	the host or a MFRC522's internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full
3	CollErr	1	a bit-collision is detected cleared automatically at receiver start-up phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd
2	CRCErr	1	the RxModeReg register's RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase
1	ParityErr	1	parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A/MIFARE communication at 106 kBd
0	ProtocolErr	1	set to logic 1 if the SOF is incorrect automatically cleared during receiver start-up phase bit is only valid for 106 kBd during the MFAuthent command, the ProtocolErr bit is set to logic 1 if the number of bytes received in one data stream is incorrect

[1] Command execution clears all error bits except the TempErr bit. Cannot be set by software.

9.3.1.8 Status1Reg register

Contains status bits of the CRC, interrupt and FIFO buffer.

Table 35. Status1Reg register (address 07h); reset value: 21h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	CRCOk	CRCReady	IRq	TRunning	reserved	HiAlert	LoAlert
Access	-	R	R	R	R	-	R	R

Table 36. Status1Reg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	CRCOk	1	the CRC result is zero for data transmission and reception, the CRCOk bit is undefined: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1
5	CRCReady	1	the CRC calculation has finished only valid for the CRC coprocessor calculation using the CalcCRC command
4	IRq	-	indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers
3	TRunning	1	MFRC522's timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock **Remark:** in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register's TGated[1:0] bits; this bit is not influenced by the gated signal
2	reserved	-	reserved for future use
1	HiAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ example: FIFO length = 60, WaterLevel = 4 $\rightarrow$ HiAlert = 1 FIFO length = 59, WaterLevel = 4 $\rightarrow$ HiAlert = 0
0	LoAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $LoAlert = FIFOLength \leq WaterLevel$ example: FIFO length = 4, WaterLevel = 4 $\rightarrow$ LoAlert = 1 FIFO length = 5, WaterLevel = 4 $\rightarrow$ LoAlert = 0

9.3.1.9 Status2Reg register

Contains status bits of the receiver, transmitter and data mode detector.

Table 37. Status2Reg register (address 08h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TempSensClear	I²CForceHS	reserved		MFCrypto1On	ModemState[2:0]		
Access	R/W	R/W	-		D	R		

Table 38. Status2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TempSensClear	1	clears the temperature error if the temperature is below the alarm limit of 125 °C
6	I²CForceHS		I²C-bus input filter settings:
		1	the I²C-bus input filter is set to the High-speed mode independent of the I²C-bus protocol
		0	the I²C-bus input filter is set to the I²C-bus protocol used
5 to 4	reserved	-	reserved
3	MFCrypto1On	-	indicates that the MIFARE Crypto1 unit is switched on and therefore all data communication with the card is encrypted can only be set to logic 1 by a successful execution of the MFAuthent command only valid in Read/Write mode for MIFARE standard cards this bit is cleared by software
2 to 0	ModemState[2:0]	-	shows the state of the transmitter and receiver state machines:
		000	idle
		001	wait for the BitFramingReg register's StartSend bit
		010	TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for TxWait is defined by the TxWaitReg register
		011	transmitting
		100	RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for RxWait is defined by the RxWaitReg register
		101	wait for data
		110	receiving

9.3.1.10 FIFODataReg register

Input and output of 64 byte FIFO buffer.

Table 39. FIFODataReg register (address 09h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData[7:0]							
Access	D							

Table 40. FIFODataReg register bit descriptions

Bit	Symbol	Description
7 to 0	FIFOData[7:0]	data input and output port for the internal 64-byte FIFO buffer FIFO buffer acts as parallel in/parallel out converter for all serial data stream inputs and outputs

9.3.1.11 FIFOLevelReg register

Indicates the number of bytes stored in the FIFO.

Table 41. FIFOLevelReg register (address 0Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FlushBuffer	FIFOLevel[6:0]						
Access	W	R						

Table 42. FIFOLevelReg register bit descriptions

Bit	Symbol	Value	Description
7	FlushBuffer	1	immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit reading this bit always returns 0
6 to 0	FIFOLevel [6:0]	-	indicates the number of bytes stored in the FIFO buffer writing to the FIFODataReg register increments and reading decrements the FIFOLevel value

9.3.1.12 WaterLevelReg register

Defines the level for FIFO under- and overflow warning.

Table 43. WaterLevelReg register (address 0Bh); reset value: 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		WaterLevel[5:0]					
Access	-		R/W					

Table 44. WaterLevelReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	WaterLevel [5:0]	defines a warning level to indicate a FIFO buffer overflow or underflow: Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel bytes Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel bytes in the FIFO buffer **Remark:** to calculate values for HiAlert and LoAlert see Section 9.3.1.8 on page 42.

9.3.1.13 ControlReg register

Miscellaneous control bits.

Table 45. ControlReg register (address 0Ch); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	reserved			RxLastBits[2:0]		
Access	W	W	-			R		

Table 46. ControlReg register bit descriptions

Bit	Symbol	Value	Description
7	TStopNow	1	timer stops immediately reading this bit always returns it to logic0
6	TStartNow	1	timer starts immediately reading this bit always returns it to logic 0
5 to 3	reserved	-	reserved for future use
2 to 0	RxLastBits[2:0]	-	indicates the number of valid bits in the last received byte if this value is 000b, the whole byte is valid

9.3.1.14 BitFramingReg register

Adjustments for bit-oriented frames.

Table 47. BitFramingReg register (address 0Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign[2:0]			reserved	TxLastBits[2:0]		
Access	W	R/W			-	R/W		

Table 48. BitFramingReg register bit descriptions

Bit	Symbol	Value	Description
7	StartSend	1	starts the transmission of data only valid in combination with the Transceive command
6 to 4	RxAlign[2:0]		used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example:
		0	LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1
		1	LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2
		7	LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0 These bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0
3	reserved	-	reserved for future use
2 to 0	TxLastBits[2:0]	-	used for transmission of bit oriented frames: defines the number of bits of the last byte that will be transmitted 000b indicates that all bits of the last byte will be transmitted

9.3.1.15 CollReg register

Defines the first bit-collision detected on the RF interface.

Table 49. CollReg register (address 0Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ValuesAfterColl	reserved	CollPosNotValid	CollPos[4:0]				
Access	R/W	-	R	R				

Table 50. CollReg register bit descriptions

Bit	Symbol	Value	Description
7	ValuesAfterColl	0	all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1
6	reserved	-	reserved for future use
5	CollPosNotValid	1	no collision detected or the position of the collision is out of the range of CollPos[4:0]

Table 50. CollReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
4 to 0	CollPos[4:0]	-	shows the bit position of the first detected collision in a received frame only data bits are interpreted example:
		00h	indicates a bit-collision in the 32nd bit
		01h	indicates a bit-collision in the 1st bit
		08h	indicates a bit-collision in the 8th bit These bits will only be interpreted if the CollPosNotValid bit is set to logic 0

9.3.1.16 Reserved register 0Fh

Functionality is reserved for future use.

Table 51. Reserved register (address 0Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 52. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

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9.3.2.1 Reserved register 10h

Functionality is reserved for future use.

Table 53. Reserved register (address 10h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 54. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.2 ModeReg register

Defines general mode settings for transmitting and receiving.

Table 55. ModeReg register (address 11h); reset value: 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	reserved	TxWaitRF	reserved	PolMFin	reserved	CRCPreset[1:0]	
Access	R/W	-	R/W	-	R/W	-	R/W	

Table 56. ModeReg register bit descriptions

Bit	Symbol	Value	Description
7	MSBFirst	1	CRC coprocessor calculates the CRC with MSB first in the CRCResultReg register the values for the CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed **Remark:** during RF communication this bit is ignored
6	reserved	-	reserved for future use
5	TxWaitRF	1	transmitter can only be started if an RF field is generated
4	reserved	-	reserved for future use
3	PolMFin		defines the polarity of pin MFIN **Remark:** the internal envelope signal is encoded active LOW, changing this bit generates a MFinActIRq event
		1	polarity of pin MFIN is active HIGH
		0	polarity of pin MFIN is active LOW
2	reserved	-	reserved for future use
1 to 0	CRCPreset [1:0]		defines the preset value for the CRC coprocessor for the CalcCRC command **Remark:** during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers
		00	0000h
		01	6363h
		10	A671h
		11	FFFFh

9.3.2.3 TxModeReg register

Defines the data rate during transmission.

Table 57. TxModeReg register (address 12h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	TxSpeed[2:0]			InvMod	reserved		
Access	R/W	D			R/W	-		

Table 58. TxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TxCRCEn	1	enables CRC generation during data transmission **Remark:** can only be set to logic 0 at 106 kBd
6 to 4	TxSpeed[2:0]		defines the bit rate during data transmission the MFRC522 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	InvMod	1	modulation of transmitted data is inverted
2 to 0	reserved	-	reserved for future use

9.3.2.4 RxModeReg register

Defines the data rate during reception.

Table 59. RxModeReg register (address 13h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RxCRCEn	RxSpeed[2:0]			RxNoErr	RxMultiple	reserved	
Access	R/W	D			R/W	R/W	-	

Table 60. RxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	RxCRCEn	1	enables the CRC calculation during reception **Remark:** can only be set to logic 0 at 106 kBd
6 to 4	RxSpeed[2:0]		defines the bit rate while receiving data the MFRC522 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	RxNoErr	1	an invalid received data stream (less than 4 bits received) will be ignored and the receiver remains active

Table 60. RxModeReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
2	RxMultiple	0	receiver is deactivated after receiving a data frame
		1	able to receive more than one data frame only valid for data rates above 106 kBd in order to handle the polling command after setting this bit the Receive and Transceive commands will not terminate automatically. Multiple reception can only be deactivated by writing any command (except the Receive command) to the CommandReg register, or by the host clearing the bit if set to logic 1, an error byte is added to the FIFO buffer at the end of a received data stream which is a copy of the ErrorReg register value. For the MFRC522 version 2.0 the CRC status is reflected in the signal CRCOk, which indicates the actual status of the CRC coprocessor. For the MFRC522 version 1.0 the CRC status is reflected in the signal CRCErr.
1 to 0	reserved	-	reserved for future use

9.3.2.5 TxControlReg register

Controls the logical behavior of the antenna driver pins TX1 and TX2.

Table 61. TxControlReg register (address 14h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2RF On	InvTx1RF On	InvTx2RF Off	InvTx1RF Off	Tx2CW	reserved	Tx2RFEn	Tx1RFEn
Access	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W

Table 62. TxControlReg register bit descriptions

Bit	Symbol	Value	Description
7	InvTx2RFOn	1	output signal on pin TX2 inverted when driver TX2 is enabled
6	InvTx1RFOn	1	output signal on pin TX1 inverted when driver TX1 is enabled
5	InvTx2RFOff	1	output signal on pin TX2 inverted when driver TX2 is disabled
4	InvTx1RFOff	1	output signal on pin TX1 inverted when driver TX1 is disabled
3	Tx2CW	1	output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier
		0	Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier
2	reserved	-	reserved for future use
1	Tx2RFEn	1	output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data
0	Tx1RFEn	1	output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data

9.3.2.6 TxASKReg register

Controls transmit modulation settings.

Table 63. TxASKReg register (address 15h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	Force100ASK	reserved					
Access	-	R/W	-					

Table 64. TxASKReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	Force100ASK	1	forces a 100 % ASK modulation independent of the ModGsPReg register setting
5 to 0	reserved	-	reserved for future use

9.3.2.7 TxSelReg register

Selects the internal sources for the analog module.

Table 65. TxSelReg register (address 16h); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		DriverSel[1:0]		MFOutSel[3:0]			
Access:	-		R/W		R/W			

Table 66. TxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5 to 4	DriverSel [1:0]	-	selects the input of drivers TX1 and TX2
		00	3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode
		01	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		10	modulation signal (envelope) from pin MFIN
		11	HIGH; the HIGH level depends on the setting of bits InvTx1RFOn/InvTx1RFOff and InvTx2RFOn/InvTx2RFOff

Table 66. TxSelReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
3 to 0	MFOutSel [3:0]		selects the input for pin MFOUT
		0000	3-state
		0001	LOW
		0010	HIGH
		0011	test bus signal as defined by the TestSel1Reg register's TstBusBitSel[2:0] value
		0100	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		0101	serial data stream to be transmitted, data stream before Miller encoder
		0110	reserved
		0111	serial data stream received, data stream after Manchester decoder
		1000 to 1111	reserved

9.3.2.8 RxSelReg register

Selects internal receiver settings.

Table 67. RxSelReg register (address 17h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UARTSel[1:0]		RxWait[5:0]					
Access	R/W		R/W					

Table 68. RxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	UARTSel [1:0]		selects the input of the contactless UART
		00	constant LOW
		01	Manchester with subcarrier from pin MFIN
		10	modulated signal from the internal analog module, default
		11	NRZ coding without subcarrier from pin MFIN which is only valid for transfer speeds above 106 kBd
5 to 0	RxWait [5:0]	-	after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this 'frame guard time' any signal on pin RX is ignored this parameter is ignored by the Receive command all other commands, such as Transceive, MFAuthent use this parameter the counter starts immediately after the external RF field is switched on

9.3.2.9 RxThresholdReg register

Selects thresholds for the bit decoder.

Table 69. RxThresholdReg register (address 18h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel[3:0]				reserved	CollLevel[2:0]		
Access	R/W				-	R/W		

Table 70. RxThresholdReg register bit descriptions

Bit	Symbol	Description
7 to 4	MinLevel [3:0]	defines the minimum signal strength at the decoder input that will be accepted if the signal strength is below this level it is not evaluated
3	reserved	reserved for future use
2 to 0	CollLevel [2:0]	defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit

9.3.2.10 DemodReg register

Defines demodulator settings.

Table 71. DemodReg register (address 19h); reset value: 4Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AddIQ[1:0]		FixIQ	TPrescal Even	TauRcv[1:0]		TauSync[1:0]	
Access	R/W		R/W	R/W	R/W		R/W	

Table 72. DemodReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	AddIQ [1:0]	-	defines the use of I and Q channel during reception **Remark:** the FixIQ bit must be set to logic 0 to enable the following settings:
		00	selects the stronger channel
		01	selects the stronger channel and freezes the selected channel during communication
		10	reserved
		11	reserved
5	FixIQ	1	if AddIQ[1:0] are set to X0b, the reception is fixed to I channel if AddIQ[1:0] are set to X1b, the reception is fixed to Q channel

Table 72. DemodReg register bit descriptions *…continued*

Bit	Symbol	Value	Description
4	TPrescalEven	R/W	Available on RC522 version 1.0 and version 2.0: If set to logic 0 the following formula is used to calculate the timer frequency of the prescaler: f_{timer} = 13.56 MHz / (2*TPreScaler+1). Only available on version 2.0: If set to logic 1 the following formula is used to calculate the timer frequency of the prescaler: f_{timer} = 13.56 MHz / (2*TPreScaler+2). Default TPrescalEven bit is logic 0, find more information on the prescaler in Section 8.5.
3 to 2	TauRcv[1:0]	-	changes the time-constant of the internal PLL during data reception **Remark:** if set to 00b the PLL is frozen during data reception
1 to 0	TauSync[1:0]	-	changes the time-constant of the internal PLL during burst

9.3.2.11 Reserved register 1Ah

Functionality is reserved for future use.

Table 73. Reserved register (address 1Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 74. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.12 Reserved register 1Bh

Functionality is reserved for future use.

Table 75. Reserved register (address 1Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 76. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.13 MfTxReg register

Controls some MIFARE communication transmit parameters.

Table 77. MfTxReg register (address 1Ch); reset value: 62h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						TxWait[1:0]	
Access	-						R/W	

Table 78. MfTxReg register bit descriptions

Bit	Symbol	Description
7 to 2	reserved	reserved for future use
1 to 0	TxWait	defines the additional response time 7 bits are added to the value of the register bit by default

9.3.2.14 MfRxReg register

Table 79. MfRxReg register (address 1Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ParityDisable	reserved			
Access	-			R/W	-			

Table 80. MfRxReg register bit descriptions

Bit	Symbol	Value	Description
7 to 5	reserved	-	reserved for future use
4	ParityDisable	1	generation of the parity bit for transmission and the parity check for receiving is switched off the received parity bit is handled like a data bit
3 to 0	reserved	-	reserved for future use

9.3.2.15 Reserved register 1Eh

Functionality is reserved for future use.

Table 81. Reserved register (address 1Eh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 82. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.16 SerialSpeedReg register

Selects the speed of the serial UART interface.

Table 83. SerialSpeedReg register (address 1Fh); reset value: EBh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BR_T0[2:0]			BR_T1[4:0]				
Access	R/W			R/W				

Table 84. SerialSpeedReg register bit descriptions

Bit	Symbol	Description
7 to 5	BR_T0[2:0]	factor BR_T0 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 12
4 to 0	BR_T1[4:0]	factor BR_T1 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 12

9.3.3 Page 2: Configuration

9.3.3.1 Reserved register 20h

Functionality is reserved for future use.

Table 85. Reserved register (address 20h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access	reserved							

Table 86. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.2 CRCResultReg registers

Shows the MSB and LSB values of the CRC calculation.

Remark: The CRC is split into two 8-bit registers.

Table 87. CRCResultReg (higher bits) register (address 21h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB[7:0]							
Access	R							

Table 88. CRCResultReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultMSB [7:0]	shows the value of the CRCResultReg register's most significant byte only valid if Status1Reg register's CRCReady bit is set to logic 1

Table 89. CRCResultReg (lower bits) register (address 22h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB[7:0]							
Access	R							

Table 90. CRCResultReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultLSB [7:0]	shows the value of the least significant byte of the CRCResultReg register only valid if Status1Reg register's CRCReady bit is set to logic 1

9.3.3.3 Reserved register 23h

Functionality is reserved for future use.

Table 91. Reserved register (address 23h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 92. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.4 ModWidthReg register

Sets the modulation width.

Table 93. ModWidthReg register (address 24h); reset value: 26h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth[7:0]							
Access	R/W							

Table 94. ModWidthReg register bit descriptions

Bit	Symbol	Description
7 to 0	ModWidth[7:0]	defines the width of the Miller modulation as multiples of the carrier frequency (ModWidth + 1 / f_{clk}) the maximum value is half the bit period

9.3.3.5 Reserved register 25h

Functionality is reserved for future use.

Table 95. Reserved register (address 25h); reset value: 87h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 96. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.6 RFCfgReg register

Configures the receiver gain.

Table 97. RFCfgReg register (address 26h); reset value: 48h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	RxGain[2:0]			reserved			
Access	-	R/W			-			

Table 98. RFCfgReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6 to 4	RxGain [2:0]		defines the receiver's signal voltage gain factor:
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	reserved	-	reserved for future use

9.3.3.7 GsNReg register

Defines the conductance of the antenna driver pins TX1 and TX2 for the n-driver when the driver is switched on.

Table 99. GsNReg register (address 27h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CWGsN[3:0]				ModGsN[3:0]			
Access	R/W				R/W			

Table 100. GsNReg register bit descriptions

Bit	Symbol	Description
7 to 4	CWGsN [3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the output power and subsequently current consumption and operating distance **Remark:** the conductance value is binary-weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on
3 to 0	ModGsN [3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the modulation index **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on

9.3.3.8 CWGsPReg register

Defines the conductance of the p-driver output during periods of no modulation.

Table 101. CWGsPReg register (address 28h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		CWGsP[5:0]					
Access	-		R/W					

Table 102. CWGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	CWGsP[5:0]	defines the conductance of the p-driver output which can be used to regulate the output power and subsequently current consumption and operating distance **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1

9.3.3.9 ModGsPReg register

Defines the conductance of the p-driver output during modulation.

Table 103. ModGsPReg register (address 29h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		ModGsP[5:0]					
Access	-		R/W					

Table 104. ModGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	ModGsP[5:0]	defines the conductance of the p-driver output during modulation which can be used to regulate the modulation index **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 if the TxASKReg register's Force100ASK bit is set to logic 1 the value of ModGsP has no effect

9.3.3.10 TModeReg and TPrescalerReg registers

These registers define the timer settings.

Remark: The TPrescaler setting higher 4 bits are in the TModeReg register and the lower 8 bits are in the TPrescalerReg register.

Table 105. TModeReg register (address 2Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TAuto	TGated[1:0]		TAutoRestart	TPrescaler_Hi[3:0]			
Access	R/W	R/W		R/W	R/W			

Table 106. TModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TAuto	1	timer starts automatically at the end of the transmission in all communication modes at all speeds if the RxModeReg register's RxMultiple bit is not set, the timer stops immediately after receiving the 5th bit (1 start bit, 4 data bits) if the RxMultiple bit is set to logic 1 the timer never stops, in which case the timer can be stopped by setting the ControlReg register's TStopNow bit to logic 1
		0	indicates that the timer is not influenced by the protocol
6 to 5	TGated[1:0]		internal timer is running in gated mode **Remark:** in gated mode, the Status1Reg register's TRunning bit is logic 1 when the timer is enabled by the TModeReg register's TGated[1:0] bits this bit does not influence the gating signal
		00	non-gated mode
		01	gated by pin MFIN
		10	gated by pin AUX1
		11	-
4	TAutoRestart	1	timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero
		0	timer decrements to 0 and the ComIrqReg register's TimerIRq bit is set to logic 1
3 to 0	TPrescaler_Hi[3:0]	-	defines the higher 4 bits of the TPrescaler value The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit in Demot Regis set to logic 0: f_{timer} = 13.56 MHz / (2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0) The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 1: f_{timer} = 13.56 MHz / (2*TPreScaler+2). See Section 8.5 "Timer unit".

Table 107. TPrescalerReg register (address 2Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TPrescaler_Lo[7:0]							
Access	R/W							

Table 108. TPrescalerReg register bit descriptions

Bit	Symbol	Description
7 to 0	TPrescaler_Lo[7:0]	defines the lower 8 bits of the TPrescaler value The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 0: f_{timer} = 13.56 MHz / (2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0) The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit inDemoReg is set to logic 1: f_{timer} = 13.56 MHz / (2*TPreScaler+2). See Section 8.5 "Timer unit".

9.3.3.11 TReloadReg register

Defines the 16-bit timer reload value.

Remark: The reload value bits are contained in two 8-bit registers.

Table 109. TReloadReg (higher bits) register (address 2Ch); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Hi[7:0]							
Access	R/W							

Table 110. TReloadReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Hi[7:0]	defines the higher 8 bits of the 16-bit timer reload value on a start event, the timer loads the timer reload value changing this register affects the timer only at the next start event

Table 111. TReloadReg (lower bits) register (address 2Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Lo[7:0]							
Access	R/W							

Table 112. TReloadReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Lo[7:0]	defines the lower 8 bits of the 16-bit timer reload value on a start event, the timer loads the timer reload value changing this register affects the timer only at the next start event

9.3.3.12 TCounterValReg register

Contains the timer value.

Remark: The timer value bits are contained in two 8-bit registers.

Table 113. TCounterValReg (higher bits) register (address 2Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Hi[7:0]							
Access	R							

Table 114. TCounterValReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Hi [7:0]	timer value higher 8 bits

Table 115. TCounterValReg (lower bits) register (address 2Fh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Lo[7:0]							
Access	R							

Table 116. TCounterValReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Lo [7:0]	timer value lower 8 bits

9.3.4 Page 3: Test

9.3.4.1 Reserved register 30h

Functionality is reserved for future use.

Table 117. Reserved register (address 30h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 118. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.4.2 TestSel1Reg register

General test signal configuration.

Table 119. TestSel1Reg register (address 31h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					TstBusBitSel[2:0]		
Access	-					R/W		

Table 120. TestSel1Reg register bit descriptions

Bit	Symbol	Description
7 to 3	reserved	reserved for future use
2 to 0	TstBusBitSel [2:0]	selects a test bus signal which is output at pin MFOUT if AnalogSelAux2[3:0] = FFh in AnalogTestReg register, test bus signal is also output at pins AUX1 or AUX2

9.3.4.3 TestSel2Reg register

General test signal configuration and PRBS control.

Table 121. TestSel2Reg register (address 32h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15	TestBusSel[4:0]				
Access	R/W	R/W	R/W	R/W				

Table 122. TestSel2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TstBusFlip	1	test bus is mapped to the parallel port in the following order: TstBusBit4,TstBusBit3, TstBusBit2, TstBusBit6, TstBusBit5, TstBusBit0; see Section 16.1 on page 82
6	PRBS9	-	starts and enables the PRBS9 sequence according to ITU-TO150 **Remark:** all relevant registers to transmit data must be configured before entering PRBS9 mode the data transmission of the defined sequence is started by the Transmit command
5	PRBS15	-	starts and enables the PRBS15 sequence according to ITU-TO150 **Remark:** all relevant registers to transmit data must be configured before entering PRBS15 mode the data transmission of the defined sequence is started by the Transmit command
4 to 0	TestBusSel[4:0]	-	selects the test bus; see Section 16.1 “Test signals”

9.3.4.4 TestPinEnReg register

Enables the test bus pin output driver.

Table 123. TestPinEnReg register (address 33h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RS232LineEn	TestPinEn[5:0]						reserved
Access	R/W	R/W						-

Table 124. TestPinEnReg register bit descriptions

Bit	Symbol	Value	Description
7	RS232LineEn	0	serial UART lines MX and DTRQ are disabled
6 to 1	TestPinEn [5:0]	-	enables the output driver on one of the data pins D1 to D7 which outputs a test signal **Example:** setting bit 1 to logic 1 enables pin D1 output setting bit 5 to logic 1 enables pin D5 output **Remark:** If the SPI is used, only pins D1 to D4 can be used. If the serial UART interface is used and the RS232LineEn bit is set to logic 1 only pins D1 to D4 can be used.
0	reserved	-	reserved for future use

9.3.4.5 TestPinValueReg register

Defines the HIGH and LOW values for the test port D1 to D7 when it is used as I/O.

Table 125. TestPinValueReg register (address 34h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UseIO	TestPinValue[5:0]						reserved
Access	R/W	R/W						-

Table 126. TestPinValueReg register bit descriptions

Bit	Symbol	Value	Description
7	UseIO	1	enables the I/O functionality for the test port when one of the serial interfaces is used the input/output behavior is defined by value TestPinEn[5:0] in the TestPinEnReg register the value for the output behavior is defined by TestPinValue[5:0]
6 to 1	TestPinValue [5:0]	-	defines the value of the test port when it is used as I/O and each output must be enabled by TestPinEn[5:0] in the TestPinEnReg register **Remark:** Reading the register indicates the status of pins D6 to D1 if the UseIO bit is set to logic 1. If the UseIO bit is set to logic 0, the value of the TestPinValueReg register is read back.
0	reserved	-	reserved for future use

9.3.4.6 TestBusReg register

Shows the status of the internal test bus.

Table 127. TestBusReg register (address 35h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TestBus[7:0]							
Access	R							

Table 128. TestBusReg register bit descriptions

Bit	Symbol	Description
7 to 0	TestBus[7:0]	shows the status of the internal test bus the test bus is selected using the TestSel2Reg register; see Section 16.1 on page 82

9.3.4.7 AutoTestReg register

Controls the digital self-test.

Table 129. AutoTestReg register (address 36h); reset value: 40h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	AmpRcv	RFT		SelfTest[3:0]			
Access	-	R/W	-		R/W			

Table 130. AutoTestReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for production tests
6	AmpRcv	1	internal signal processing in the receiver chain is performed non-linearly which increases the operating distance in communication modes at 106 kBd **Remark:** due to non-linearity, the effect of the RxThresholdReg register's MinLevel[3:0] and the CollLevel[2:0] values is also non-linear
5 to 4	RFT	-	reserved for production tests
3 to 0	SelfTest[3:0]	-	enables the digital self test the self test can also be started by the CalcCRC command; see Section 10.3.1.4 on page 71 the self test is enabled by value 1001b **Remark:** for default operation the self test must be disabled by value 0000b

9.3.4.8 VersionReg register

Shows the MFRC522 software version.

Table 131. VersionReg register (address 37h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Version[7:0]							
Access	R							

Table 132. VersionReg register bit descriptions

Bit	Symbol	Description
7 to 4	Chiptype	'9' stands for MFRC522
3 to 0	Version	'1' stands for MFRC522 version 1.0 and '2' stands for MFRC522 version 2.0.

MFRC522 version 1.0 software version is: 91h.

MFRC522 version 2.0 software version is: 92h.

9.3.4.9 AnalogTestReg register

Determines the analog output test signal at, and status of, pins AUX1 and AUX2.

Table 133. AnalogTestReg register (address 38h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AnalogSelAux1[3:0]				AnalogSelAux2[3:0]			
Access	R/W				R/W			

Table 134. AnalogTestReg register bit descriptions

Bit	Symbol	Value	Description
7 to 4	AnalogSelAux1 [3:0]		controls pin AUX1
		0000	3-state
		0001	output of TestDAC1 (AUX1), output of TestDAC2 (AUX2)[1]
		0010	test signal Corr1[1]
		0011	reserved
		0100	DAC: test signal MinLevel[1]
		0101	DAC: test signal ADC_I[1]
		0110	DAC: test signal ADC_Q[1]
		0111	reserved
		1000	reserved, test signal for production test[1]
		1001	reserved
		1010	HIGH
		1011	LOW
		1100	TxActive: at 106 kBd: HIGH during Start bit, Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1101	RxActive: at 106 kBd: HIGH during Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1110	subcarrier detected: 106 kBd: not applicable 212 kBd: 424 kBd and 848 kBd: HIGH during last part of data and CRC
		1111	test bus bit as defined by the TestSel1Reg register's TstBusBitSel[2:0] bits **Remark:** all test signals are described in Section 16.1 on page 82
3 to 0	AnalogSelAux2 [3:0]	-	controls pin AUX2 (see bit descriptions for AUX1)

[1] **Remark:** Current source output; the use of 1 kΩ pull-down resistor on AUXn is recommended.

9.3.4.10 TestDAC1Reg register

Defines the test value for TestDAC1.

Table 135. TestDAC1Reg register (address 39h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC1[5:0]					
Access	-		R/W					

Table 136. TestDAC1Reg register bit descriptions

Bit	Symbol	Description
7	reserved	reserved for production tests
6	reserved	reserved for future use
5 to 0	TestDAC1[5:0]	defines the test value for TestDAC1 output of DAC1 can be routed to AUX1 by setting value AnalogSelAux1[3:0] to 0001b in the AnalogTestReg register

9.3.4.11 TestDAC2Reg register

Defines the test value for TestDAC2.

Table 137. TestDAC2Reg register (address 3Ah); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC2[5:0]					
Access	-		R/W					

Table 138. TestDAC2Reg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	TestDAC2[5:0]	defines the test value for TestDAC2 output of DAC2 can be routed to AUX2 by setting value AnalogSelAux2[3:0] to 0001b in the AnalogTestReg register

9.3.4.12 TestADCReg register

Shows the values of ADC I and Q channels.

Table 139. TestADCReg register (address 3Bh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ADC_I[3:0]				ADC_Q[3:0]			
Access	R				R			

Table 140. TestADCReg register bit descriptions

Bit	Symbol	Description
7 to 4	ADC_I[3:0]	ADC I channel value
3 to 0	ADC_Q[3:0]	ADC Q channel value

9.3.4.13 Reserved register 3Ch

Functionality reserved for production test.

Table 141. Reserved register (address 3Ch); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 142. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 143. Reserved register (address 3Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 144. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 145. Reserved register (address 3Eh); reset value: 03h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 146. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 147. Reserved register (address 3Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 148. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

10. MFRC522 command set

10.1 General description

The MFRC522 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see Table 149) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

10.2 General behavior

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

10.3 MFRC522 command overview

Table 149. Command overview

Command	Command code	Action
Idle	0000	no action, cancels current command execution
Mem	0001	stores 25 bytes into the internal buffer
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self test
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
-	1101	reserved for future use
MFAuthent	1110	performs the MIFARE standard authentication as a reader
SoftReset	1111	resets the MFRC522

10.3.1 MFRC522 command descriptions

10.3.1.1 Idle

Places the MFRC522 in Idle mode. The Idle command also terminates itself.

10.3.1.2 Mem

Transfers 25 bytes from the FIFO buffer to the internal buffer.

To read out the 25 bytes from the internal buffer the Mem command must be started with an empty FIFO buffer. In this case, the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power-down (using pin NRSTPD), the 25 bytes in the internal buffer remain unchanged and are only lost if the power supply is removed from the MFRC522.

This command automatically terminates when finished and the Idle command becomes active.

10.3.1.3 Generate RandomID

This command generates a 10-byte random number which is initially stored in the internal buffer. This then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the MFRC522 returns to Idle mode.

10.3.1.4 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts.

This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the MFRC522 enters Self Test mode. Starting the CalcCRC command initiates a digital self test. The result of the self test is written to the FIFO buffer.

10.3.1.5 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

10.3.1.6 NoCmdChange

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

10.3.1.7 Receive

The MFRC522 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command will not automatically terminate. It must be terminated by starting another command in the CommandReg register.

10.3.1.8 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to logic 1. This command must be cleared by writing any command to the CommandReg register.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

10.3.1.9 MFAuthent

This command manages MIFARE authentication to enable a secure communication to any MIFARE Mini, MIFARE 1K and MIFARE 4K card. The following data is written to the FIFO buffer before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes are written to the FIFO.

Remark: When the MFAuthent command is active all access to the FIFO buffer is blocked. However, if there is access to the FIFO buffer, the ErrorReg register's WrErr bit is set.

This command automatically terminates when the MIFARE card is authenticated and the Status2Reg register's MFCrypto1On bit is set to logic 1.

This command does not terminate automatically if the card does not answer, so the timer must be initialized to automatic mode. In this case, in addition to the IdleIRq bit, the TimerIRq bit can be used as the termination criteria. During authentication processing, the RxIRq bit and TxIRq bit are blocked. The Crypto1On bit is only valid after termination of the MFAuthent command, either after processing the protocol or writing Idle to the CommandReg register.

If an error occurs during authentication, the ErrorReg register's ProtocolErr bit is set to logic 1 and the Status2Reg register's Crypto1On bit is set to logic 0.

10.3.1.10 SoftReset

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

Remark: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kBd.

11. Limiting values

Table 150. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.5	+4.0	V
V_{DDD}	digital supply voltage		–0.5	+4.0	V
$V_{DD(PVDD)}$	PVDD supply voltage		–0.5	+4.0	V
$V_{DD(TVDD)}$	TVDD supply voltage		–0.5	+4.0	V
$V_{DD(SVDD)}$	SVDD supply voltage		–0.5	+4.0	V
V_I	input voltage	all input pins except pins MFIN and RX	$V_{SS(PVSS)}$ – 0.5	$V_{DD(PVDD)}$ + 0.5	V
		pin MFIN	$V_{SS(PVSS)}$ – 0.5	$V_{DD(SVDD)}$ + 0.5	V
P_{tot}	total power dissipation	per package; and V_{DDD} in shortcut mode	-	200	mW
T_j	junction temperature		-	100	°C
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
		MM; 0.75 μH, 200 pF; JESD22-A114-A	-	200	V
		Charged device model; JESD22-C101-A			
		on all pins	-	200	V
		on all pins except SVDD in TFBGA64 package	-	500	V

12. Recommended operating conditions

Table 151. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
T_{amb}	ambient temperature	HVQFN32		–25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance (the achievable operating distance).

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

13. Thermal characteristics

Table 152. Thermal characteristics

Symbol	Parameter	Conditions		Package	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB		HVQFN32	40	K/W

14. Characteristics

Table 153. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input characteristics							
Pins EA, I2C and NRSTPD							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
Pin MFIN							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(SVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(SVDD)}$	V
Pin SDA							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
Pin RX[1]							
V_i	input voltage			–1	-	V_{DDA} +1	V
C_i	input capacitance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset		-	10	-	pF
R_i	input resistance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset		-	350	-	Ω
Input voltage range; see Figure 24							
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V		-	100	-	mV
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V		-	4	-	V
Input sensitivity; see Figure 24							
V_{mod}	modulation voltage	minimum Manchester encoded; V_{DDA} = 3 V; RxGain[2:0] = 111b (48 dB)		-	5	-	mV
Pin OSCIN							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DDA}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDA}$	V

Table 153. Characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance	V_{DDA} = 2.8 V; DC = 0.65 V; AC = 1 V (p-p)		-	2	-	pF
Input/output characteristics							
pins D1, D2, D3, D4, D5, D6 and D7							
I_{LI}	input leakage current			−1	-	+1	μA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
Output characteristics							
Pin MFOUT							
V_{OH}	HIGH-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(SVDD)}$ − 0.4	-	$V_{DD(SVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(SVDD)}$ = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(SVDD)}$ = 3 V		-	-	4	mA
Pin IRQ							
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
Pins AUX1 and AUX2							
V_{OH}	HIGH-level output voltage	V_{DDD} = 3 V; I_O = 4 mA		V_{DDD} − 0.4	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	V_{DDD} = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	V_{DDD} = 3 V		-	-	4	mA
Pins TX1 and TX2							

Table 153. Characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.15	-	-	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.4	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.24	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.64	-	-	V
V_{OL}	LOW-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.15	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.4	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.24	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.64	V
Current consumption							
I_{pd}	power-down current	V_{DDA} = V_{DDD} = $V_{DD(TVDD)}$ = $V_{DD(PVDD)}$ = 3 V					
		hard power-down; pin NRSTPD set LOW	[2]	-	-	5	µA
		soft power-down; RF level detector on	[2]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; V_{DDD} = 3 V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V; CommandReg register's bit RcvOff = 0		-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} = 3 V; CommandReg register's bit RcvOff = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[3]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[4][5][6]	-	60	100	mA
$I_{DD(SVDD)}$	SVDD supply current	pin SVDD	[7]	-	-	4	mA
Clock frequency							
f_{clk}	clock frequency			-	27.12	-	MHz
δ_{clk}	clock duty cycle			40	50	60	%
t_{jit}	jitter time	RMS		-	-	10	ps
Crystal oscillator							

Table 153. Characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	pin OSCOUT		-	1.1	-	V
V_{OL}	LOW-level output voltage	pin OSCOUT		-	0.2	-	V
C_i	input capacitance	pin OSCOUT		-	2	-	pF
		pin OSCIN		-	2	-	pF
Typical input requirements							
f_{xtal}	crystal frequency			-	27.12	-	MHz
ESR	equivalent series resistance			-	-	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	50	100	mW

[1] The voltage on pin RX is clamped by internal diodes to pins AVSS and AVDD.

[2] I_{pd} is the total current for all supplies.

[3] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[4] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[5] During typical circuit operation, the overall current is below 100 mA.

[6] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

[7] $I_{DD(SVDD)}$ depends on the load at pin MFOUT.

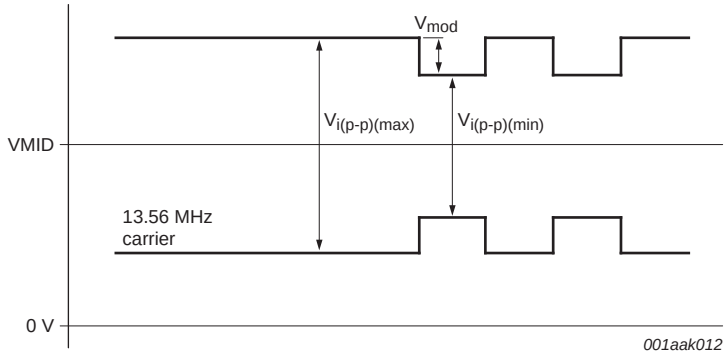


Fig 24. Pin RX input voltage range

14.1 Timing characteristics

Table 154. SPI timing characteristics

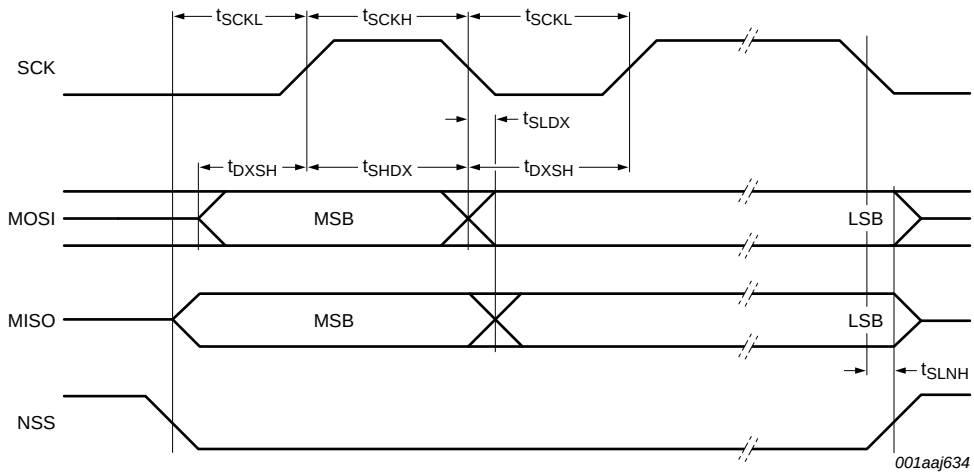
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WL}	pulse width LOW	line SCK		50	-	-	ns
t_{WH}	pulse width HIGH	line SCK		50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI		25	-	-	ns

Table 154. SPI timing characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK		25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO		-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time			0	-	-	ns
t_{NHNL}	NSS high before communication			50	-	-	ns

Table 155. I^2C-bus timing in Fast mode

Symbol	Parameter	Conditions	Fast mode		High-speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	400	0	3400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	after this period, the first clock pulse is generated	600	-	160	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	160	-	ns
$t_{SU;STO}$	set-up time for STOP condition		600	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock		600	-	60	-	ns
$t_{HD;DAT}$	data hold time		0	900	0	70	ns
$t_{SU;DAT}$	data set-up time		100	-	10	-	ns
t_r	rise time	SCL signal	20	300	10	40	ns
t_f	fall time	SCL signal	20	300	10	40	ns
t_r	rise time	SDA and SCL signals	20	300	10	80	ns
t_f	fall time	SDA and SCL signals	20	300	10	80	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	1.3	-	µs



Remark: The signal NSS must be LOW to be able to send several bytes in one data stream. To send more than one data stream NSS must be set HIGH between the data streams.

Fig 25. Timing diagram for SPI

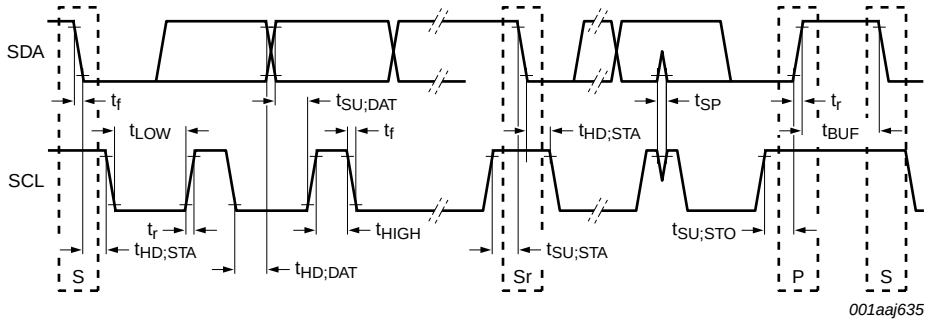


Fig 26. Timing for Fast and Standard mode devices on the I^2C-bus

15. Application information

A typical application diagram using a complementary antenna connection to the MFRC522 is shown in Figure 27.

The antenna tuning and RF part matching is described in the application note Ref. 1 and Ref. 2.

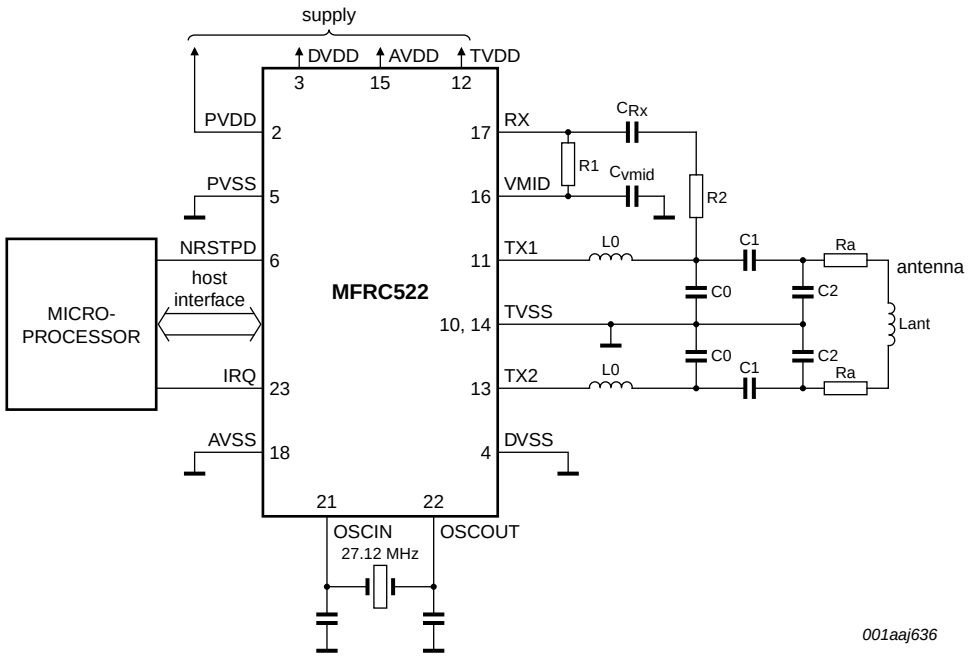


Fig 27. Typical application diagram

16. Test information

16.1 Test signals

16.1.1 Self test

The MFRC522 has the capability to perform a digital self test. The self test is started by using the following procedure:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and implement the Config command.
3. Enable the self test by writing 09h to the AutoTestReg register.
4. Write 00h to the FIFO buffer.
5. Start the self test with the CalcCRC command.
6. The self test is initiated.
7. When the self test has completed, the FIFO buffer contains the following 64 bytes:

FIFO buffer byte values for MFRC522 version 1.0:

00h, C6h, 37h, D5h, 32h, B7h, 57h, 5Ch,
C2h, D8h, 7Ch, 4Dh, D9h, 70h, C7h, 73h,
10h, E6h, D2h, AAh, 5Eh, A1h, 3Eh, 5Ah,
14h, AFh, 30h, 61h, C9h, 70h, DBh, 2Eh,
64h, 22h, 72h, B5h, BDh, 65h, F4h, ECh,
22h, BCh, D3h, 72h, 35h, CDh, AAh, 41h,
1Fh, A7h, F3h, 53h, 14h, DEh, 7Eh, 02h,
D9h, 0Fh, B5h, 5Eh, 25h, 1Dh, 29h, 79h

FIFO buffer byte values for MFRC522 version 2.0:

00h, EBh, 66h, BAh, 57h, BFh, 23h, 95h,
D0h, E3h, 0Dh, 3Dh, 27h, 89h, 5Ch, DEh,
9Dh, 3Bh, A7h, 00h, 21h, 5Bh, 89h, 82h,
51h, 3Ah, EBh, 02h, 0Ch, A5h, 00h, 49h,
7Ch, 84h, 4Dh, B3h, CCh, D2h, 1Bh, 81h,
5Dh, 48h, 76h, D5h, 71h, 061h, 21h, A9h,
86h, 96h, 83h, 38h, CFh, 9Dh, 5Bh, 6Dh,
DCh, 15h, BAh, 3Eh, 7Dh, 95h, 03Bh, 2Fh

16.1.2 Test bus

The test bus is used for production tests. The following configuration can be used to improve the design of a system using the MFRC522. The test bus allows internal signals to be routed to the digital interface. The test bus comprises two sets of test signals which are selected using their subaddress specified in the TestSel2Reg register's TestBusSel[4:0] bits. The test signals and their related digital output pins are described in Table 156 and Table 157.

Table 156. Test bus signals: TestBusSel[4:0] = 07h

Pins	Internal signal name	Description
D6	s_data	received data stream
D5	s_coll	bit-collision detected (106 kBd only)
D4	s_valid	s_data and s_coll signals are valid
D3	s_over	receiver has detected a stop condition
D2	RCV_reset	receiver is reset
D1	-	reserved

Table 157. Test bus signals: TestBusSel[4:0] = 0Dh

Pins	Internal test signal name	Description
D6	clkstable	oscillator output signal
D5	clk27/8	oscillator output signal divided by 8
D4 to D3	-	reserved
D2	clk27	oscillator output signal
D1	-	reserved

16.1.3 Test signals on pins AUX1 or AUX2

The MFRC522 allows the user to select internal signals for measurement on pins AUX1 or AUX2. These measurements can be helpful during the design-in phase to optimize the design or used for test purposes.

Table 158 shows the signals that can be switched to pin AUX1 or AUX2 by setting AnalogSelAux1[3:0] or AnalogSelAux2[3:0] in the AnalogTestReg register.

Remark: The DAC has a current output, therefore it is recommended that a 1 kΩ pull-down resistor is connected to pin AUX1 or AUX2.

Table 158. Test signal descriptions

AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value	Signal on pin AUX1 or pin AUX2
0000	3-state
0001	DAC: register TestDAC1 or TestDAC2
0010	DAC: test signal Corr1
0011	reserved
0100	DAC: test signal MinLevel
0101	DAC: test signal ADC_I
0110	DAC: test signal ADC_Q
0111 to 1001	reserved
1010	HIGH
1011	LOW
1100	TxActive

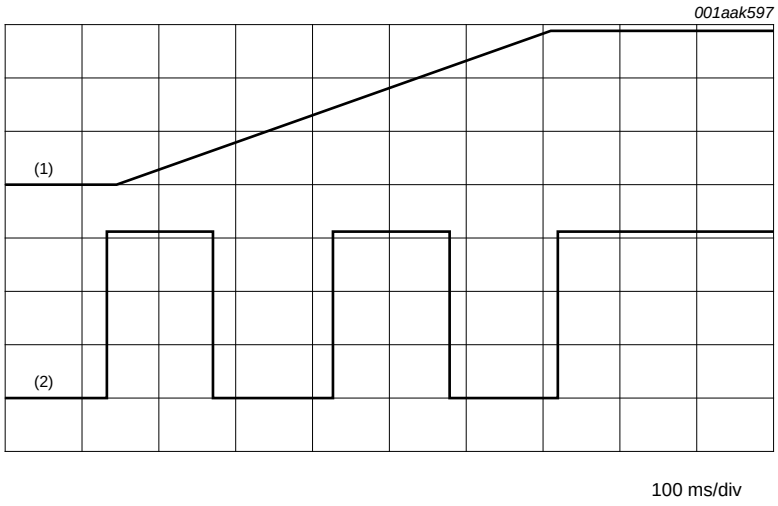
Table 158. Test signal descriptions *...continued*

AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value	Signal on pin AUX1 or pin AUX2
1101	RxActive
1110	subcarrier detected
1111	TstBusBit

16.1.3.1 Example: Output test signals TestDAC1 and TestDAC2

The AnalogTestReg register is set to 11h. The output on pin AUX1 has the test signal TestDAC1 and the output on pin AUX2 has the test signal TestDAC2. The signal values of TestDAC1 and TestDAC2 are controlled by the TestDAC1Reg and TestDAC2Reg registers.

Figure 28 shows test signal TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2 when the TestDAC1Reg register is programmed with a slope defined by values 00h to 3Fh and the TestDAC2Reg register is programmed with a rectangular signal defined by values 00h and 3Fh.

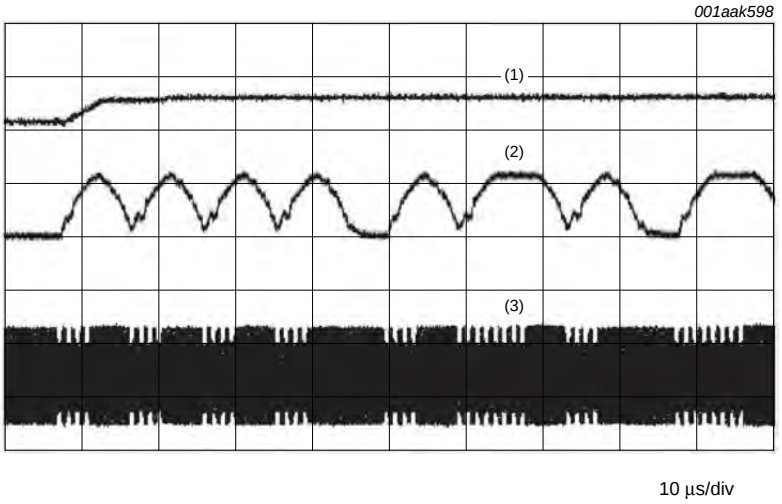


(1) TestDAC1 (500 mV/div) on pin AUX1.
(2) TestDAC2 (500 mV/div) on pin AUX2.

Fig 28. Output test signals TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2

16.1.3.2 Example: Output test signals Corr1 and MinLevel

Figure 29 shows test signals Corr1 and MinLevel on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 24h.

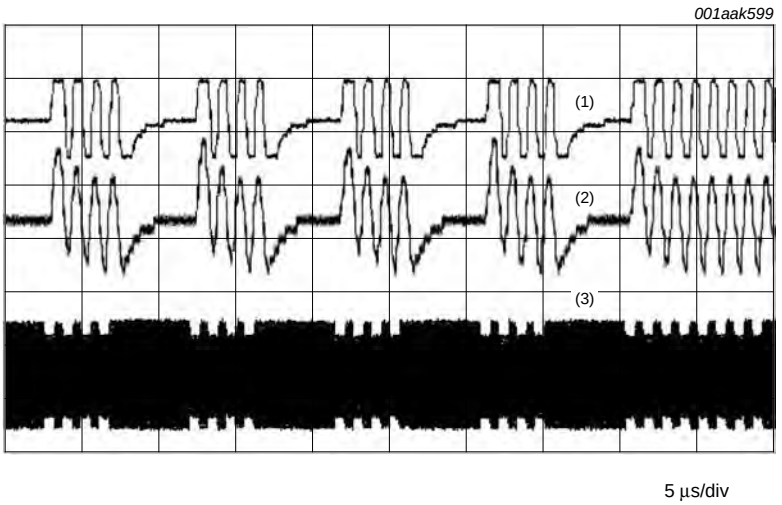


(1) MinLevel (1 V/div) on pin AUX2.
(2) Corr1 (1 V/div) on pin AUX1.
(3) RF field.

Fig 29. Output test signals Corr1 on pin AUX1 and MinLevel on pin AUX2

16.1.3.3 Example: Output test signals ADC channel I and ADC channel Q

Figure 30 shows the channel behavior test signals ADC_I and ADC_Q on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 56h.



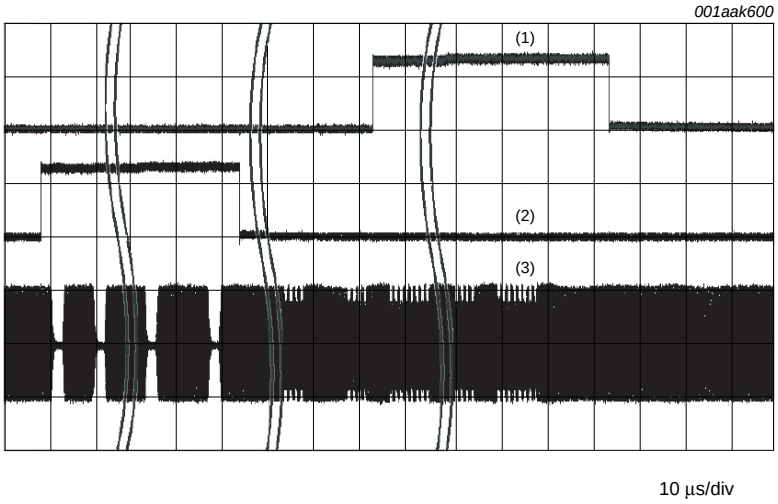
(1) ADC_I (1 V/div) on pin AUX1.
(2) ADC_Q (500 mV/div) on pin AUX2.
(3) RF field.

Fig 30. Output ADC channel I on pin AUX1 and ADC channel Q on pin AUX2

16.1.3.4 Example: Output test signals RxActive and TxActive

Figure 31 shows the RxActive and TxActive test signals relating to RF communication. The AnalogTestReg register is set to CDh.

- At 106 kBd, RxActive is HIGH during data bits, parity and CRC reception. Start bits are not included
- At 106 kBd, TxActive is HIGH during start bits, data bits, parity and CRC transmission
- At 212 kBd, 424 kBd and 848 kBd, RxActive is HIGH during data bits and CRC reception. Start bits are not included
- At 212 kBd, 424 kBd and 848 kBd, TxActive is HIGH during data bits and CRC transmission

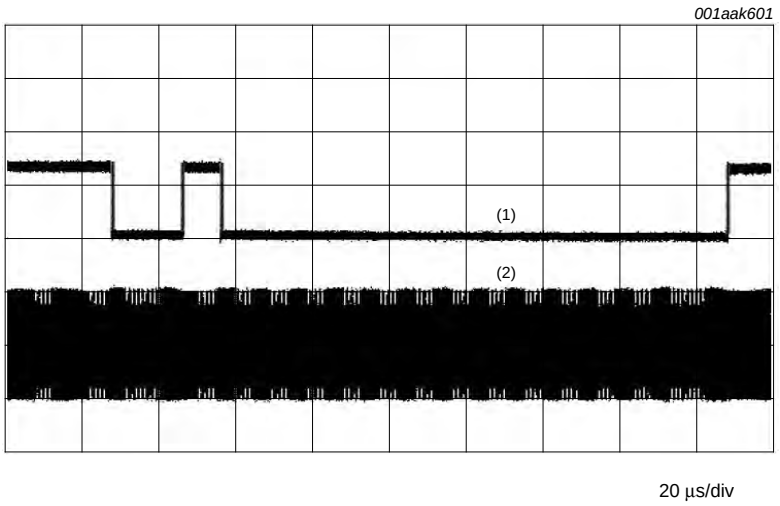


(1) RxActive (2 V/div) on pin AUX1.
(2) TxActive (2 V/div) on pin AUX2.
(3) RF field.

Fig 31. Output RxActive on pin AUX1 and TxActive on pin AUX2

16.1.3.5 Example: Output test signal RX data stream

Figure 32 shows the data stream that is currently being received. The TestSel2Reg register's TestBusSel[4:0] bits are set to 07h to enable test bus signals on pins D1 to D6; see Section 16.1.2 on page 82. The TestSel1Reg register's TstBusBitSel[2:0] bits are set to 06h (pin D6 = s_data) and AnalogTestReg register is set to FFh (TstBusBit) which outputs the received data stream on pins AUX1 and AUX2.



(1) s_data (received data stream) (2 V/div).

(2) RF field.

Fig 32. Received data stream on pins AUX1 and AUX2

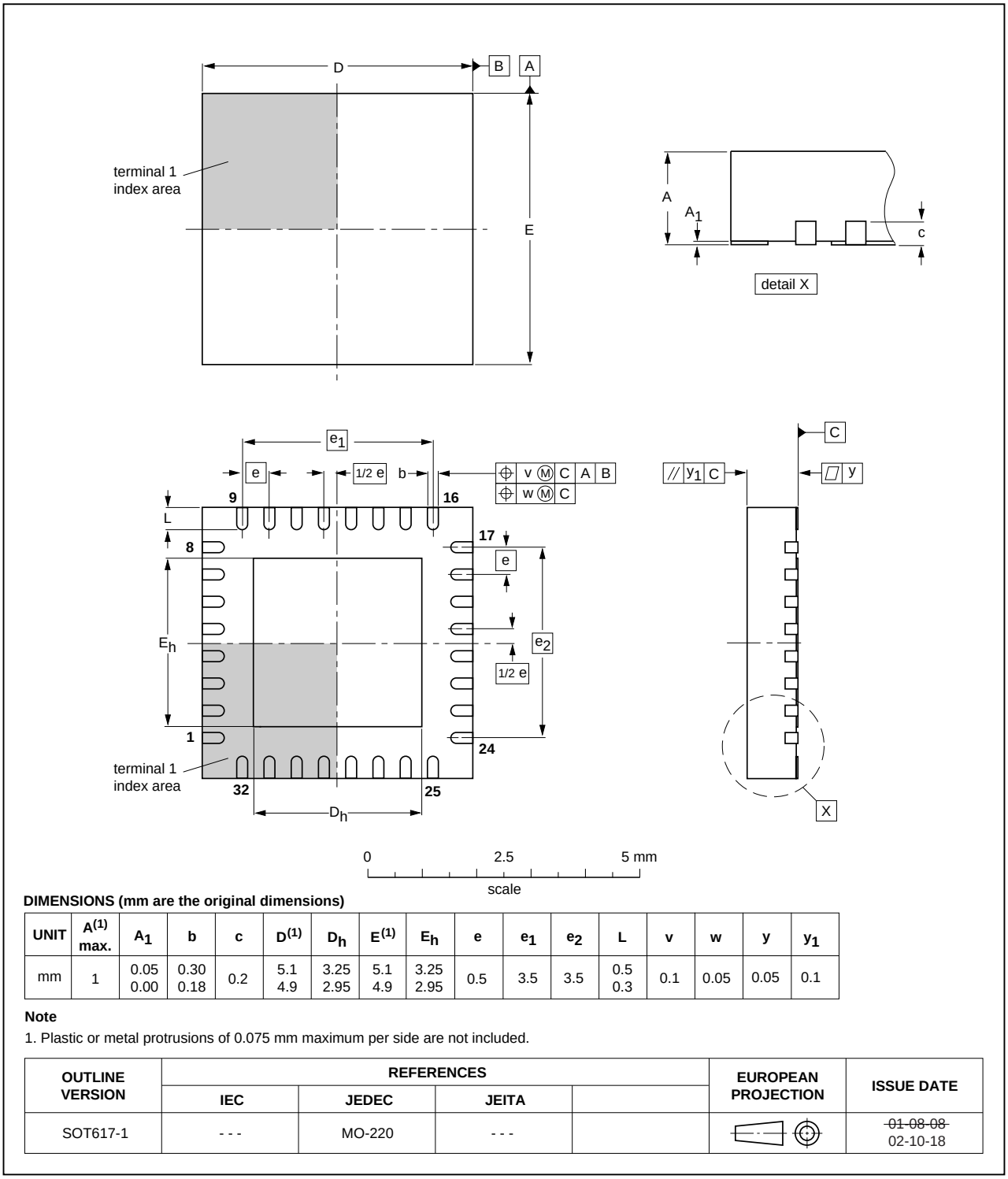
16.1.3.6 PRBS

The pseudo-random binary sequences PRBS9 and PRBS15 are based on ITU-TO150 and are defined with the TestSel2Reg register. Transmission of either data stream is started by the Transmit command. The preamble/sync byte/start bit/parity bit are automatically generated depending on the mode selected.

Remark: All relevant registers for transmitting data must be configured in accordance with ITU-TO150 before selecting PRBS transmission.

17. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 33. Package outline SOT617-1 (HVQFN32)

Detailed package information can be found at:
http://www.nxp.com/package/SOT617-1.html.

18. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*. MSL for this package is level 1 which means 260 °C convection reflow temperature.

Dry pack is not required.

Unlimited out-of-pack floor life at maximum ambient 30 °C/85 % RH.

19. Packing information

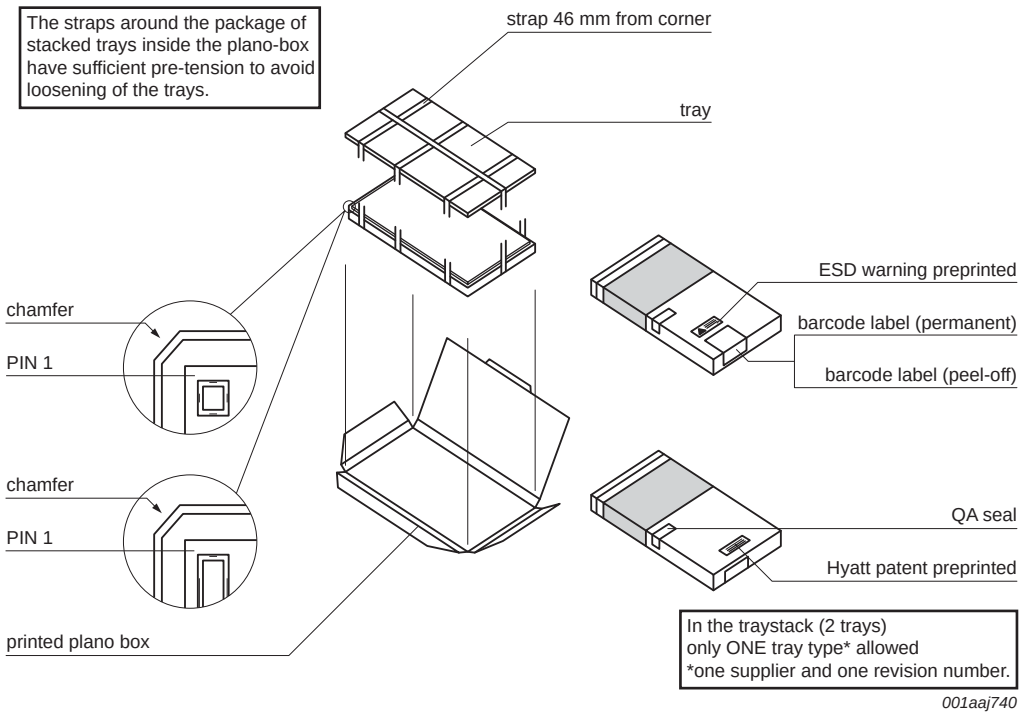


Fig 34. Packing information 1 tray

20. Abbreviations

Table 159. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital-to-Analog Converter
HBM	Human Body Model
I^2C	Inter-integrated Circuit
LSB	Least Significant Bit
MISO	Master In Slave Out
MM	Machine Model
MOSI	Master Out Slave In
MSB	Most Significant Bit
NRZ	Not Return to Zero
NSS	Not Slave Select
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

21. References

[1] **Application note —** *MFRC52x Reader IC Family Directly Matched Antenna Design*

[2] **Application note —** *MIFARE (ISO/IEC 14443 A) 13.56 MHz RFID Proximity Antennas*

22. Revision history

Table 160. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MFRC522 v.3.9	20160427	Product data sheet	-	MFRC522 v.3.8
Modifications:	• Section 1 “Introduction” and Section 2 “General description”: updated and NTAG functionality added • Descriptive title updated			
MFRC522 v.3.8	20140917	Product data sheet	-	MFRC522 v.3.7
Modifications:	• Table 150 “Limiting values”: updated			
MFRC522 v.3.7	20140326	Product data sheet	-	MFRC522 v.3.6
Modifications:	• Change of descriptive title • Section 23.4 “Licenses” removed			
MFRC522 v.3.6	20111214	Product data sheet	-	MFRC522_35
Modifications:	• Section 1.1 “Differences between version 1.0 and 2.0” on page 1: added • Table 2 “Ordering information” on page 3: updated • Section 9.3.2.10 “DemodReg register” on page 53: register updated and add reference to Timer unit • Section 8.5 “Timer unit” on page 31: Pre Scaler Information for version 2.0 added • Section 9.3.4.8 “VersionReg register” on page 66: version information structured in chip information and version information updated, including version 1.0 and 2.0 • Section 16.1 “Test signals” on page 82: selftest result including values for version 1.0 and 2.0			
MFRC522_35	20100621	Product data sheet		MFRC522_34
Modifications:	• Section 9.3.2.10 “DemodReg register” on page 53: register updated • Section 9.3.3.10 “TModeReg and TPrescalerReg registers” on page 60: register updated • Section 8.5 “Timer unit” on page 31: timer calculation updated • Section 9.3.4.8 “VersionReg register” on page 66: version B2h updated • Section 16.1 “Test signals” on page 82: selftest result updated			
MFRC522_34	20100305	Product data sheet		MFRC522_33
Modifications:	• Section 8.5 “Timer unit”: information added • Table 106 “TModeReg register bit descriptions”: bit 7 updated • Table 154 “SPI timing characteristics”: row added			
MFRC522_33	20091026	Product data sheet	-	112132

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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25. Contents

continued >>

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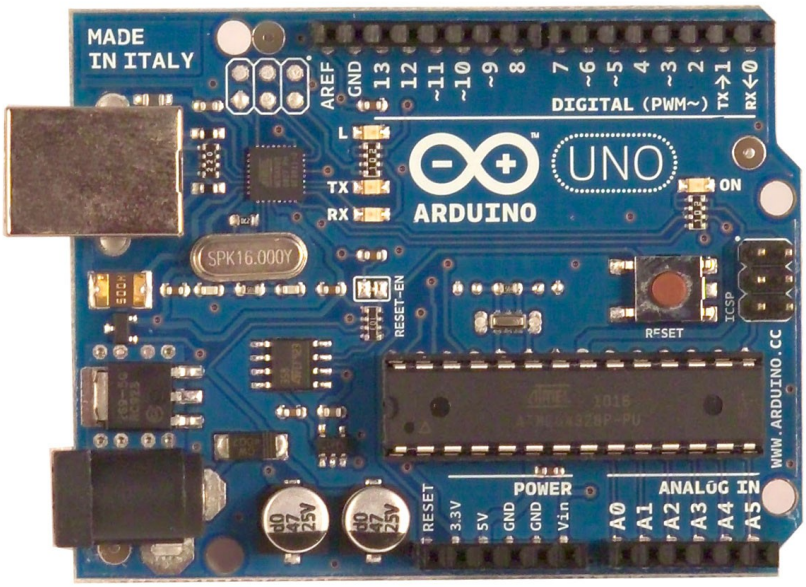
Date of release: 27 April 2016
112139

Arduino UNO



Product Overview

The Arduino Uno is a microcontroller board based on the ATmega328 (datasheet). It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started. The Uno differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter.

"Uno" means one in Italian and is named to mark the upcoming release of Arduino 1.0. The Uno and version 1.0 will be the reference versions of Arduno, moving forward. The Uno is the latest in a series of USB Arduino boards, and the reference model for the Arduino platform; for a comparison with previous versions, see the index of Arduino boards.

Index

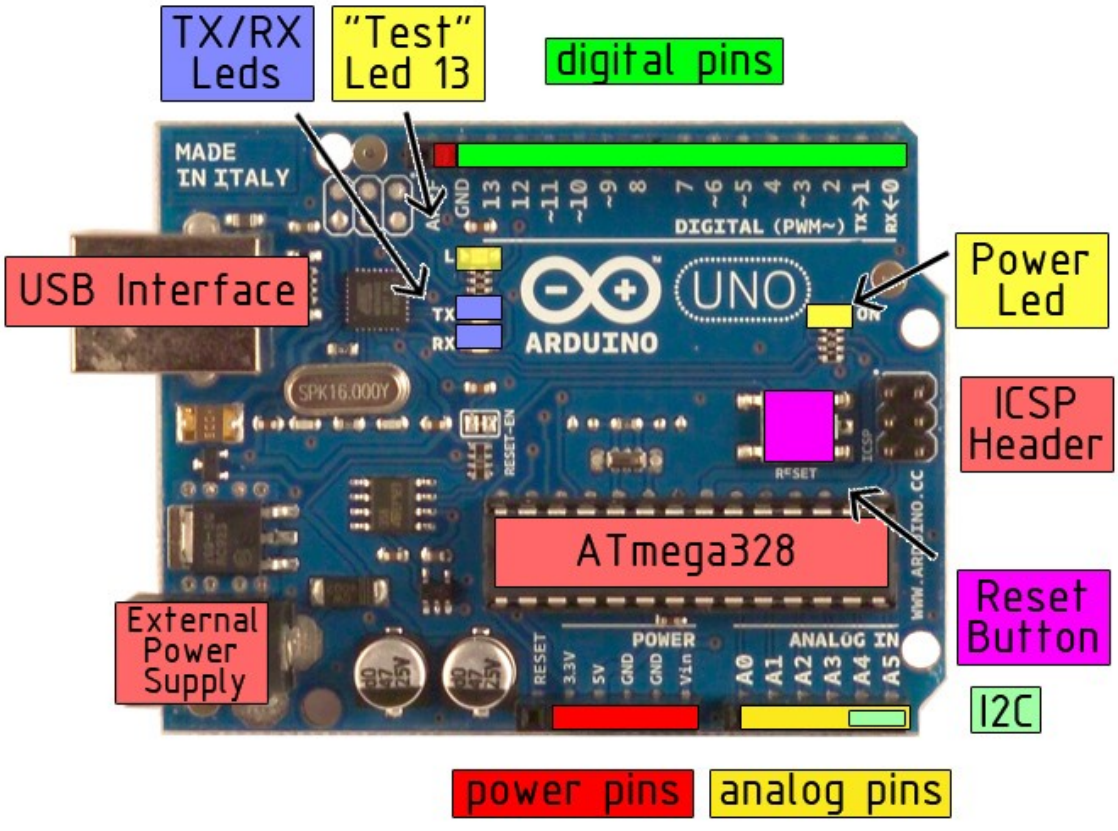
Technical Specification

EAGLE files: arduino-duemilanove-uno-design.zip Schematic: arduino-uno-schematic.pdf

Summary

Microcontroller	ATmega328
Operating Voltage	5V
Input Voltage (recommended)	7-12V
Input Voltage (limits)	6-20V
Digital I/O Pins	14 (of which 6 provide PWM output)
Analog Input Pins	6
DC Current per I/O Pin	40 mA
DC Current for 3.3V Pin	50 mA
Flash Memory	32 KB of which 0.5 KB used by bootloader
SRAM	2 KB
EEPROM	1 KB
Clock Speed	16 MHz

the board



Power

The Arduino Uno can be powered via the USB connection or with an external power supply. The power source is selected automatically.

External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The power pins are as follows:

- **VIN.** The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.
- **5V.** The regulated power supply used to power the microcontroller and other components on the board. This can come either from VIN via an on-board regulator, or be supplied by USB or another regulated 5V supply.
- **3V3.** A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.
- **GND.** Ground pins.

Memory

The Atmega328 has 32 KB of flash memory for storing code (of which 0,5 KB is used for the bootloader); It has also 2 KB of SRAM and 1 KB of EEPROM (which can be read and written with the EEPROM library).

Input and Output

Each of the 14 digital pins on the Uno can be used as an input or output, using pinMode(), digitalWrite(), and digitalRead() functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial: 0 (RX) and 1 (TX).** Used to receive (RX) and transmit (TX) TTL serial data. TThese pins are connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip .
- **External Interrupts: 2 and 3.** These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value. See the attachInterrupt() function for details.
- **PWM: 3, 5, 6, 9, 10, and 11.** Provide 8-bit PWM output with the analogWrite() function.
- **SPI: 10 (SS), 11 (MOSI), 12 (MISO), 13 (SCK).** These pins support SPI communication, which, although provided by the underlying hardware, is not currently included in the Arduino language.

- **LED: 13.** There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

The Uno has 6 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the AREF pin and the analogReference() function. Additionally, some pins have specialized functionality:

- **I²C: 4 (SDA) and 5 (SCL).** Support I²C (TWI) communication using the Wire library.

There are a couple of other pins on the board:

- **AREF.** Reference voltage for the analog inputs. Used with analogReference().
- **Reset.** Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

See also the mapping between Arduino pins and Atmega328 ports.

Communication

The Arduino Uno has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega328 provides UART TTL (5V) serial communication, which is available on digital pins 0 (RX) and 1 (TX). An ATmega8U2 on the board channels this serial communication over USB and appears as a virtual com port to software on the computer. The '8U2 firmware uses the standard USB COM drivers, and no external driver is needed. However, on Windows, an *.inf file is required..

The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the Arduino board. The RX and TX LEDs on the board will flash when data is being transmitted via the USB-to-serial chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A SoftwareSerial library allows for serial communication on any of the Uno's digital pins.

The ATmega328 also support I2C (TWI) and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus; see the documentation for details. To use the SPI communication, please see the ATmega328 datasheet.

Programming

The Arduino Uno can be programmed with the Arduino software (download). Select "Arduino Uno w/ ATmega328" from the **Tools > Board** menu (according to the microcontroller on your board). For details, see the reference and tutorials.

The ATmega328 on the Arduino Uno comes preburned with a bootloader that allows you to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol (reference, C header files).

You can also bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header; see these instructions for details.

The ATmega8U2 firmware source code is available . The ATmega8U2 is loaded with a DFU bootloader, which can be activated by connecting the solder jumper on the back of the board (near the map of Italy) and then resetting the 8U2. You can then use Atmel's FLIP software (Windows) or the DFU programmer (Mac OS X and Linux) to load a new firmware. Or you can use the ISP header with an external programmer (overwriting the DFU bootloader).

Automatic (Software) Reset

Rather than requiring a physical press of the reset button before an upload, the Arduino Uno is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2 is connected to the reset line of the ATmega328 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.

This setup has other implications. When the Uno is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Uno. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.

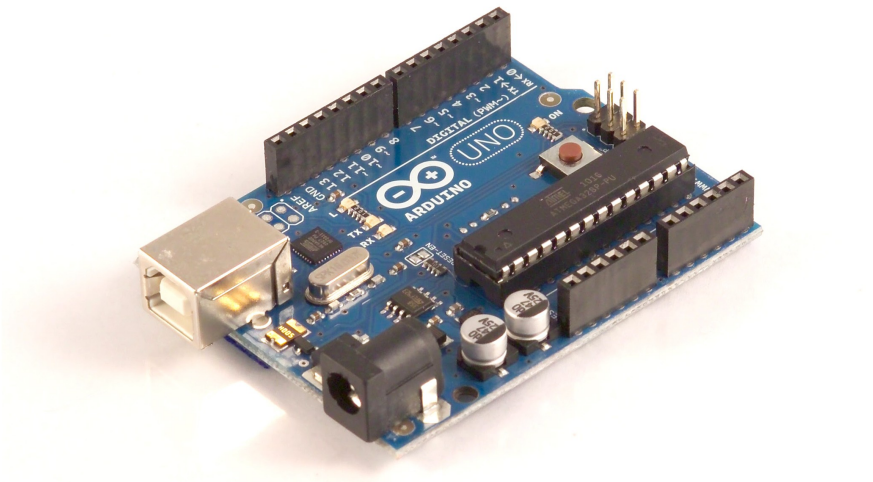
The Uno contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN". You may also be able to disable the auto-reset by connecting a 110 ohm resistor from 5V to the reset line; see this forum thread for details.

USB Overcurrent Protection

The Arduino Uno has a resettable polyfuse that protects your computer's USB ports from shorts and overcurrent. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

Physical Characteristics

The maximum length and width of the Uno PCB are 2.7 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Three screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16"), not an even multiple of the 100 mil spacing of the other pins.



How to use Arduino

Arduino can sense the environment by receiving input from a variety of sensors and can affect its surroundings by controlling lights, motors, and other actuators. The microcontroller on the board is programmed using the Arduino programming language (based on Wiring) and the Arduino development environment (based on Processing). Arduino projects can be stand-alone or they can communicate with software on running on a computer (e.g. Flash, Processing, MaxMSP).

Arduino is a cross-platoform program. You'll have to follow different instructions for your personal OS. Check on the Arduino site for the latest instructions. *http://arduino.cc/en/Guide/HomePage*

Linux Install Windows Install Mac Install

Once you have downloaded/unzipped the arduino IDE, you can Plug the Arduino to your PC via USB cable.

Blink led

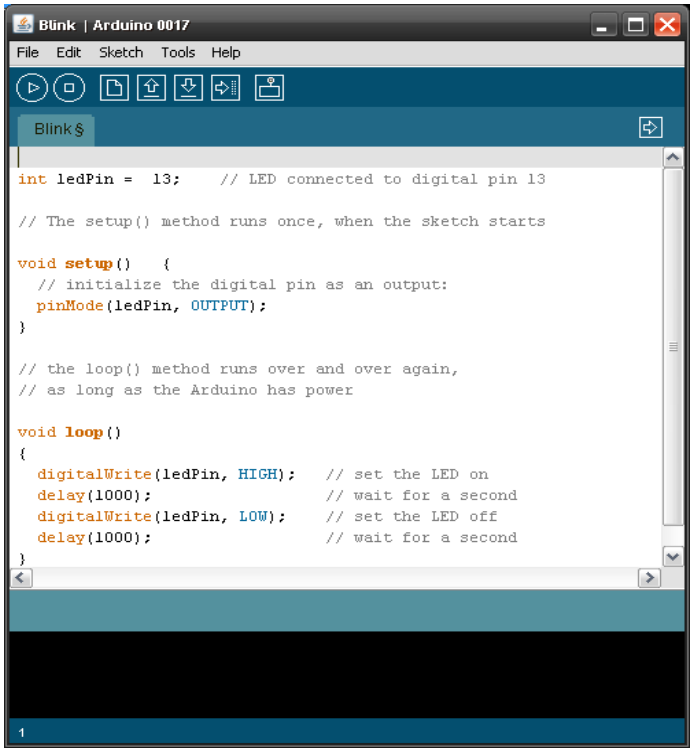
Now you're actually ready to "burn" your first program on the arduino board. To select "blink led", the physical translation of the well known programming "hello world", select

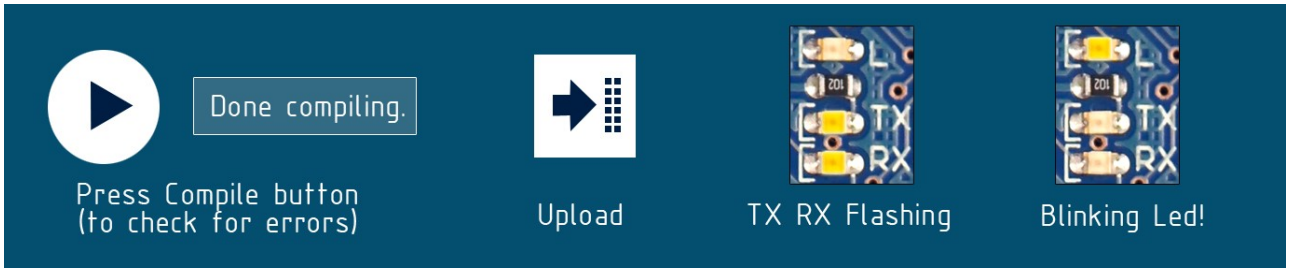
File>Sketchbook>
Arduino-0017>Examples>
Digital>Blink

Once you have your skecth you'll see something very close to the screenshot on the right.

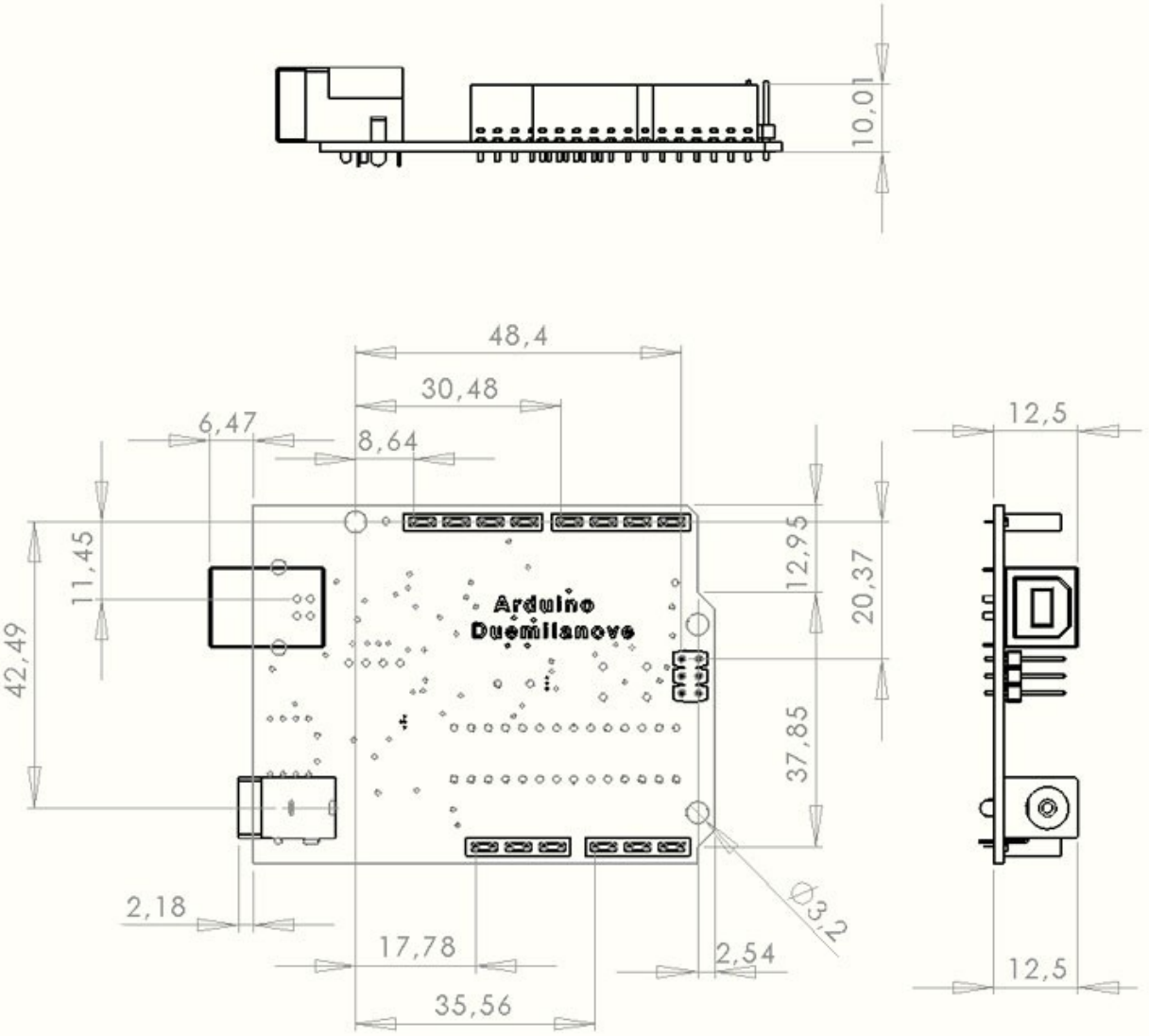
In **Tools>Board** select

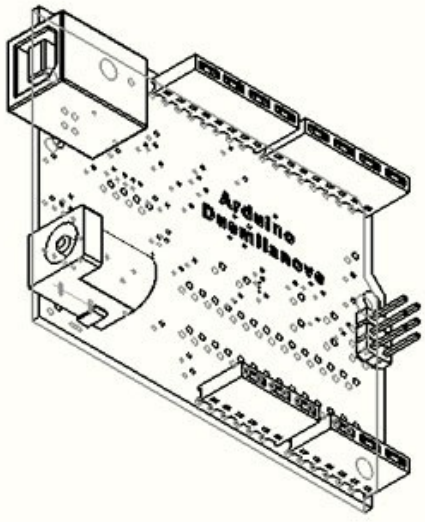
Now you have to go to
Tools>SerialPort
and select the right serial port, the one arduino is attached to.





Dimensioned Drawing





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